HIGH-PERFORMANCE MILLIMETER-WAVE AND TERAHERTZ DESIGN, A NEW APPROACH TO DESIGN ABOVE $F_{MAX}/2$

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HIGH-PERFORMANCE MILLIMETER-WAVE AND TERAHERTZ DESIGN, A NEW APPROACH TO DESIGN ABOVE $F_{MAX}/2$

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All promising applications of terahertz (THz) and millimeter-wave (mm-wave) systems, from imaging and spectroscopy to high data-rate communication, necessitate the design of high efficiency signal sources and amplifiers. In addition to the high propagation loss of the signals in these frequency ranges, the poor activity of the existing CMOS/SiGe devices working above $f_{max}/2$ emphasizes on the importance of developing new design methods in order to have high output power and efficiency signal sources and high power gain amplifiers.

Despite of these challenges in circuit design at this frequency range, the myriad applications of the systems working in this frequency range has attracted many researchers to work on these systems. In the past ten years, the reported output power of signal sources in this frequency range has increased by more than 40 dB which is a huge progress. High frequency amplifiers have also passed through a tremendous progress during the past decade. However, generating sufficient power is still one of the critical issue in these systems. Indeed, the so-called "terahertz gap" is a quite well-known fact, which means both silicon based electronics and photonics based devices are incapable of generating adequate power in the mm-wave and terahertz frequency range. Thus, the researchers have to come up with new methodologies to increase the output power. This main challenge presents itself in designing two fundamental circuit blocks that appear in most electronic systems and circuits, i.e. the signal sources and the amplifiers. Compared to low frequency, the former lacks high DC-to-RF efficiency and the latter suffers

from a low power gain.

Chapter 1 provides a complete overview of progress and challenges in mm-wave and THz signal source design. In Chapter 2 a novel approach to design efficient high-output-power fundamental oscillators beyond $f_{max}/2$ of the employed process is presented. The idea is to shape and maximize the unilateral power gain of the network at the desired frequency using optimum passive internal and external feedback networks. The proposed technique significantly improves the output power and DC-to-RF efficiency of the oscillator. To show the feasibility of this novel approach, a 175 GHz fundamental oscillator is designed in a 130 nm SiGe BiCMOS process ($f_{max} \simeq 280$ GHz), which achieves a measured DC-to-RF efficiency of 11.7% that is one of the highest ones among all previously reported oscillators above $f_{max}/3$ of their active devices. Measurements show that the designed oscillator generates a peak power of 3 mW (4.8 dBm) with a phase noise FoM of -195.4 dBc/Hz at 1 MHz offset frequency, which is the highest phase noise FoM among all reported CMOS/BiCMOS mm-wave and terahertz oscillators. The proposed method takes into account the possible PVT variations as well as modeling errors of the passive components in the design stage. A similar approach to design efficient high-output-power fundamental oscillators close to the f_{max} of the employed process is presented in Chapter 3. The idea is based on shaping and optimizing the maximally efficient power gain (G_{ME}) of the circuit using a pair of internal/external feedback mechanisms. Solving a constrained optimization problem, an optimum pair of passive feedback network is designed to achieve the highest maximally efficient power gain in order to increase the output power and thence the DC-to-RF efficiency. A 195 GHz fundamental oscillator is designed in a 55 nm SiGe process ($f_{max} \simeq 340$ GHz), which achieves a significantly higher DC-to-RF efficiency (15.3%) among all reported oscillators working above $f_{max}/3$ of their active devices. The oscillator generates a peak power of 4.5 mW (6.5 dBm) with the best phase noise of -82.3 dBc/Hz and the best FoM

of -197 dBc/Hz measured at 100 KHz offset frequency, which is the best phase noise and FoM among all CMOS/SiGe mm-Wave oscillators. The proposed optimization-based method takes into account PVT variations as well as modeling errors of all components in the design process to guarantee the functionality of the fabricated circuit.

The last two chapters address the challenging problem of designing high power gain amplifiers at mm-wave and THz frequency ranges. A novel theory of stability for two-port networks is developed in Chapter 4. Using this theory, a new method of designing amplifiers with high power gain working close to the maximum frequency of oscillation (f_{max}) is proposed. Contrary to the existing amplifier design methodologies, in this method the transistor capability of power amplification is fully utilized. This becomes more important at frequencies close to the f_{max} where having high power gain is challenging due to degraded activity of the employed device. The proposed method considers the modeling errors and process-voltage-temperature (PVT) variations of the employed components in the design stage to ensure that the fabricated amplifier will be stable with a decent power gain even if the worst case variations and modeling errors happen. To show the feasibility of the proposed approach, a three-stage amplifier at 173 GHz, using BJT's from a 130 nm SiGe process is designed. The fabricated amplifier has a maximum measured power gain of 18.5 dB at 173 GHz which achieves highest defined power gain FoM among all reported state of the arts.

Chapter 5 proposes a new approach to design a mm-wave high power gain cascode amplifier. The gain is enhanced by adjusting the size of the cascode transistor together with a desensitized inductive impedance at its base. The impedance at this node has a critical role in determining both gain and stability. The employed desensitization technique decreases the effect of process variations and modeling errors on this impedance which results in a reliable design. Providing enough degrees of freedom, this method results in a conjugate matched input and output impedances. Therefore, two or more

of this stage can be simply cascaded to get higher gain with no need for an interstage matching network and hence no additional loss and gain degradation. Based on this approach, a single stage amplifier at 183 GHz is implemented in a 130 nm SiGe process which has a power gain of 9.5 dB, 3 dB bandwidth of 8.5 GHz and saturation power of -2.8 dBm.

BIOGRAPHICAL SKETCH

Hamid Khatibi was born in 1973. He received B.Sc. in Electronics and M.Sc. in Control System from Sharif University of Technology, Tehran, Iran in 1997 and 1999 respectively. In 2004, he joined Laboratoir d'Automatique at EPFL where he accomplished a PhD in control system engineering. In 2012, he joined UNIC at Cornell, where he received his M.Sc. in Electronics in 2015 and is doing his research on high performance mm-wave circuit, convex optimization and signal integrity challenges.

During his study, he has been a recipient of several awards such as: Jacob's Scholarship (Cornell-2012), Exceptionally valuable performance prize (EPFL-2007), Honored master student (Iran-1999), Ranked first among all B.Sc. and M.Sc. students (Sharif-1997 and 1999), Best B.Sc. thesis contest (Sharif-1999), Gold medal in Physics Olympiad (1992-Iran) and Silver medal in Computer Programming Olympiad. He has taught Physics for more than ten years and has been the manager of two Special Business Units of FANAP Co. (ICT Subsidiary of PASARGAD Financial Group-Tehran-Iran). He has also been a circuit designer in several companies during 1994 to 2003. He has been the author of several papers in electronics and control system engineering.

This thesis is dedicated to whomever reads it and learns a few interesting facts from it.

ACKNOWLEDGEMENTS

I would like to thank every single person who has helped me in my life and particularly in finishing my PhD at Cornell. I cannot indicate all the names here. So, I just mention a few to show my gratitude. I would like to express my appreciation towards my advisor, Ehsan, a brother and a friend who helped me in different ways during past five years and supported me to accomplish my PhD at Cornell. I cannot forget how he helped even my family during these years. I would like to thank Prof. Molnar and Prof. Apsel with whom I passed some courses and learned basics of circuit design. I also like to thank Prof. Pollock who always disperse positive energy to the world by his smile. I would like to express my gratitude towards my friend and office-mate, Somaye, who was always there for me and helped me during the difficult moments. Without her help I would not be able to finish my study at Cornell. I would like to thank Omeed Momeni for his help in arranging some of our measurements at UC Davis and also Guansheng Li for his helpful responses to all my questions even when he had left Cornell.

At the end, I would like to thank my wife and son, Maryam and Alireza, for being with me and supporting me in all situations no matter how difficult it was. I also express my deep gratitude towards my parents who did support me in my whole life with their blessings. Last but not least, I want to show my appreciation to my former advisor at EPFL, Alireza Karimi, who opened my eyes to a new world and changed my life forever and my main advisor at EPFL, Roland Longchamp, who will be always my role model as a real human and one of the nicest persons I have ever met.

CONTENTS

LIST OF TABLES

LIST OF FIGURES

CHAPTER 1

TOWARDS EFFICIENT HIGH POWER MM-WAVE AND TERAHERTZ SOURCES IN SILICON: ONE DECADE OF PROGRESS

All promising applications of terahertz (THz) and millimeter-wave (mm-wave) systems, from imaging and spectroscopy to high data-rate communication, necessitate the design of high efficiency signal generators. In addition to the high propagation loss of the signals in these frequency ranges, the lack of activity of the current CMOS/SiGe devices (since the desired frequencies are close to their f_{max} or beyond it) emphasizes on the importance of coming up with new design methods in order to generate high output power signal sources. At UNIC group of Cornell university, we have a long history of designing mm-wave and terahertz signal generators. It started from designing oscillators close to the f_{max} with output power much higher than the state of the art oscillators in CMOS and SiGe technologies. It embarked on a 121 GHz fundamental oscillator with -3.5 dBm output power in a 130 nm CMOS process. To generate higher frequencies, harmonic generators and frequency multipliers have led to oscillators with oscillation frequencies beyond the f_{max}. For instance, a triple-push oscillator is fabricated in 65 nm CMOS process with -7.9 dBm output power at 480 GHz. In the next phase, to cope with the challenges of using varactors for frequency tuning, a novel injection-locked loop of oscillators is designed using these advanced oscillators as the core, which shows a 4.5% of tuning range at 290 GHz and has increased the output power to -2.1 dBm by combining the power of the fourth harmonic of four push-push oscillators. In another attempt, the injection-locked tuning loop is built upon eight voltage controlled oscillators (VCO's). Combining the output power of the second harmonic of the eight core VCO's leads to a maximum output power of 4.1 dBm at 256 GHz and the resulting VCO has a tuning range of 4.3% by employing two varactors, one inside the oscillator block and the other one in the phase shifter.

At this point, the maximum DC-to-RF efficiency of all these oscillators were below 1.1% which compels the next challenging step to improve the DC-to-RF efficiency to a reasonable value. In this vital step, using a completely novel idea of shaping and maximizing the unilateral power gain of a two-port network (the measure of its activity), a fundamental oscillator is designed in a 130 nm SiGe process which has improved the DC-to-RF efficiency by a factor of 10 and has increased the output power to more than 4.8 dBm, utilizing only one transistor. This new approach enables the future THz and mm-wave systems to become both efficient and also capable of producing high output power. High tunability and frequencies higher than the f_{max} in addition to much higher output power can be attained by employing previous steps of combining the output powers and tuning through injection-locked loop of oscillators.

1.1 Introduction

In recent years, terahertz and mm-wave systems have attracted many researchers because of numerous promising applications that they provide. The most fundamental block of such systems is the signal generator which needs to have high output power, low phase noise, high DC-to-RF efficiency and also a reasonable tuning range to cover both variations and the desired bandwidth. A couple of serious issues raise a strong barrier to make high output power and high DC-to-RF efficiency oscillators in these frequency ranges. First and foremost, as the frequency approaches the maximum frequency of oscillation (f_{max}), the activity of the transistors degrades. In fact, mm-wave and terahertz frequency ranges are either close, or even beyond the f_{max} of the existing SiGe and CMOS transistors. Degraded activity of the transistors results in low output power and low DC-to-RF efficiency. Activity of a two-port network can be quantified using its unilateral power gain which is adopted as the activity figure of merit (FoM) [8].

The so-called Mason's invariant, or the unilateral power gain of a transistor decreases by a slope of 20 dB/dec beyond $f_{max}/2$ and becomes unity at f_{max} [8]. On the other hand, a two-port network can oscillate only if it is unstable. Moreover, activity is a necessary condition for the instability. Thence, it is impossible to have a fundamental signal source beyond the f_{max} where the device is not active anymore, and it is very challenging to design an efficient high power oscillator close to this frequency where the activity is quite degraded. Second, the employed metalization and passive components are very lossy due to the skin effect and also because the self-resonance frequency of the passives are in these frequency ranges. That is, part of the generated power will be lost inside the circuit itself. In other words, the lossy passives decrease the activity of the entire network which can be seen as if the utilized transistors have lower f_{max}. Moreover, the quality factor of the varactors are usually close to one or even less in these frequency ranges which makes it more challenging to have a reasonable tuning range on top of the low output power and unacceptable efficiency. Finally, the electric and magnetic coupling to the lossy substrate result in substantial loss in these frequency ranges. Furthermore, similar to the silicon based electronics, photonics based systems are also incapable of generating reasonable output power since these frequency ranges are too low for them. That is why beside the myriad useful and attractive applications for mm-wave and THz systems, the existing state of the art systems are bulky, costly and mostly fabricated in expensive GaAs and InP processes. The so-called terahertz gap ([9]) is a result of the lack of ability to generate reasonable amount of power in these frequency ranges. This clarifies that employing the same design methods of radio frequency oscillators might not be a reasonable choice for mm-wave and terahertz sources and new techniques and structures are required in order to design high output power and high efficiency oscillators in these frequency ranges. Besides, since the varactors are very lossy in this frequency range, designing oscillators with reasonable tuning range is a serious issue. A

lossy varactor not only degrades the output power and efficiency of the circuit, but also cannot change the frequency as desired. As frequency increases, in addition to the degraded quality factor, the parasitics of the varactor dominate its performance resulting in smaller variation of its capacitance and hence, small tuning range. It is clear that as the output power increases for a fixed bias, the DC-to-RF efficiency improves. Namely, in contrary to the tuning range which has trade-off with both output power and phase noise (mostly due to the added loss of the varactor), DC-to-RF efficiency and output power are aligned and usually can be improved together along with the phase noise. In this note, around one-decade progress in the mm-Wave and THz oscillator and VCO design at Cornell university is summarized. The first step initiated by the design of fundamental oscillators close to the f_{max} of the employed transistors with a reasonable output power. In the next step, to increase the frequency beyond the f_{max}, two approaches are followed, harmonic generation and frequency multiplication. In the third phase, the tuning range is considered to jump from the simple oscillators to the voltage controlled oscillators (VCO's). In order not to engage lossy varactors inside the oscillator block, a loop of cascaded injection-locked oscillators with phase shifters/couplers is proposed. The proposed design leads to a power combining structure which extracts and combines the desired harmonic of all oscillators in the loop. Varactors are employed in the phase shifters to change the phase shift between the oscillators and thence the frequency. At this point, we had designed VCO's at the desired frequency range with output power of above 3 dBm and more than 4% tuning range with a reasonable phase noise. However, the DC-to-RF efficiency of none of them was beyond 1.14% which is not acceptable particularly for systems that would be driven by a battery. Besides, such an oscillator with a peak output power of 4 dBm would take an area of about 0.5 μm^2 which is not reasonable for this amount of output power. Therefore, the next step was to restart from the beginning in order to increase the efficiency to an acceptable level to become able

to commercialize systems with such circuit blocks. Back to the first step, oscillators are designed with peak output power of 4.8 dBm and DC-to-RF efficiency of 11.7% using a single transistor. Now, these new oscillators can go through the same path to provide VCO's with reasonable tuning range and even higher output power and frequency. To the best of our knowledge, the oscillators designed at UNIC group of Cornell university have beaten all records in their reporting time and have always bested the existing state of the art signal generators. In the following, a brief explanation of each step with one or two published samples are summarized.

1.2 First Step: Oscillators with High Output Power Close to f_{max}

Realization of oscillators close to the f_{max} is a challenging problem due to the degraded activity of the transistors as explained before. In order to accomplish such a difficult task, one way is to maximize the added-power, i.e. $P_R = \max\{Re(P_{out} - P_{in})\}$ [10]. However, it is shown that the added-power cannot be derived independent of the electrical variables [10,11] and hence several variants of P_R are optimized instead [1,5,11]. To increase the output power of the oscillator, instead of P_R, $G_m = P_R/|V_{in}||V_{out}|$ is optimized in [1], using the y-parameters of the transistor as a two-port network:

$$G_m = \frac{P_R}{|V_{in}||V_{out}|} = -(A^{-1}g_{11} + Ag_{22}) - |y_{12} + y_{21}^*|cos(\angle(y_{12} + y_{21}^*) + \phi), \tag{1.1}$$

where $A = |V_{out}|/|V_{in}|$ is the voltage gain and $\phi = \angle(V_{out}/V_{in})$ is its phase shift from the input to the output. As (1.1) suggests, it is not possible to maximize P_R since it is not independent of variables such as V_{in} and V_{out} and hence, G_m is optimized instead which results in

$$A_{opt} = \sqrt{g_{11}/g_{22}}$$

and

$$\phi_{opt} = (2k + 1)\pi - \angle(y_{12} + y_{21}^{*}).$$

That is, by providing this gain and phase, G_m would be maximized which in case input and output voltages be independent of the design (which is not the case), the total real power flow out of the transistor would be maximized. This idea can be employed for designing high output power oscillators at any frequency but close to the f_{max} where the activity is degraded drastically, it is more vital to have oscillators with higher output power. Based on providing this optimality conditions, a fundamental oscillator at 121 GHz is fabricated in 130 nm CMOS process which has a maximum output power of -3.5 dBm while burning 21 mW DC power (Fig. 1.1). For the employed transistor of the

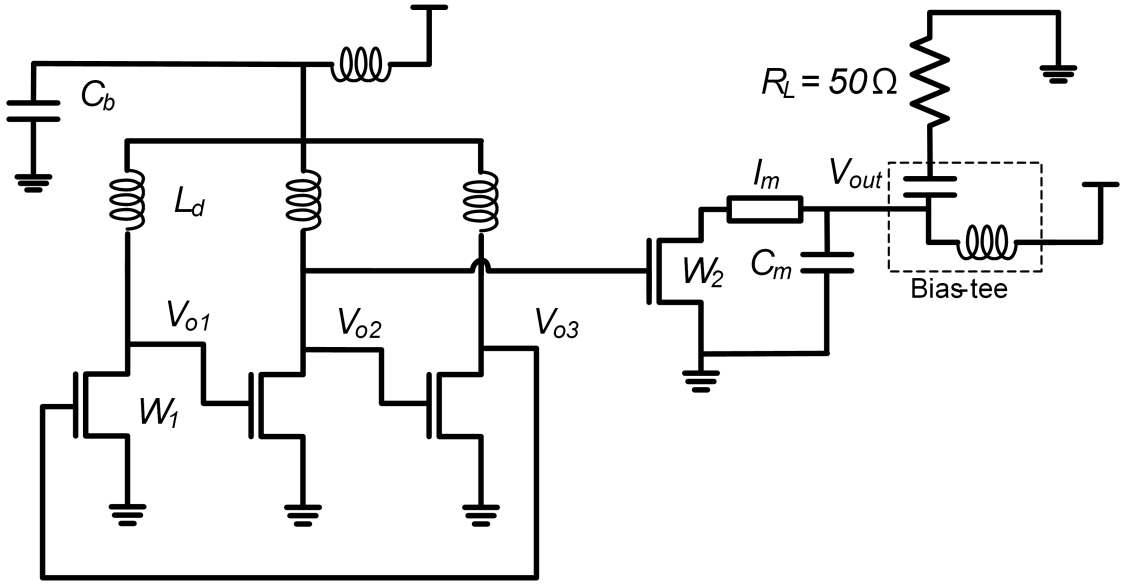

Figure 1.1: A 121 GHz fundamental oscillator [1] designed based on optimization of (1.1)

130 nm CMOS process, $A_{opt} = 1.03$ and $\phi_{opt} = 129^{\circ}$ which means that a ring oscillator composed of three similar stages which simply provides $A = 1$ and $\phi = 120^{\circ}$ is close enough to the desired optimal point (See Fig. 1.1).

1.3 Second Step: Oscillators with High Output Power Beyond f_{max}

Theoretically, beyond the f_{max} the transistor is not active and hence it is not possible to have fundamental oscillation. Unfortunately, the f_{max} has not been much improved by continuous down scaling of the CMOS transistors. This limits the fundamental oscillator design to frequencies below the f_{max}.

In order to generate power at frequencies beyond the f_{max}, the nonlinearity of a device must be utilized. To generate harmonics two choices are available. The first way is to design a harmonic oscillator and the second option is to use a frequency multiplier along with a signal generator. The frequency multiplier itself can be active or passive. However, to have a better power efficiency, passive multipliers are preferred.

1.3.1 Harmonic Oscillator

In [1], a triple push oscillator is designed using the same optimal point of (1.1) (see Fig. 1.2). It is important to excite the nonlinearity of a device as much as possible to generate more harmonic power. Although it has not been shown that increasing the fundamental generated power necessarily results in the higher harmonic generation, it seems to be one of the most reasonable choices [1]. The third harmonic is extracted from the supply common node of the ring oscillator shown in Fig. 1.2, which is implemented in a 65 nm CMOS process where the A_{opt} and ϕ_{opt} of the employed transistors at 150 GHz are 0.56 and 163° respectively. This is why an inductor is added to the gates of each transistor to push the voltage gain and phase of each transistor towards the optimum values. By a careful matching design, the power of fundamental oscillation circulates in the loop (to maximally excite the nonlinearity of the transistors), while the third harmonic power is

extracted from the common supply node using a local and global matching at the third harmonic [1].

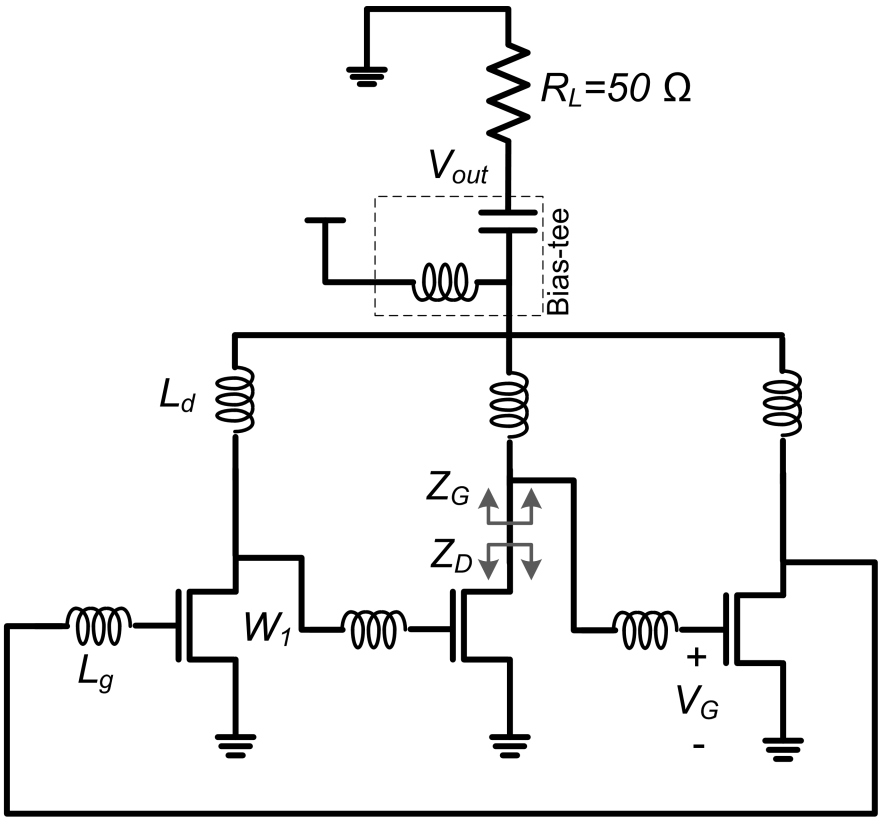

Figure 1.2: A triple push, 450 GHz harmonic oscillator [1] designed based on optimization of (1.1)

1.3.2 Frequency Multiplier

To generate power at frequencies beyond the f_{max}, an alternative to harmonic extraction is to utilize a frequency multiplier, usually driven by a fundamental oscillator. A frequency multiplier can be active [2] or passive [3]. The straightforward structure of the multipliers, which is usually based on a simple geometry, normally results in a broadband capability of such circuits compared to the harmonic generators.

An active 234 to 253 GHz doubler is proposed in [2] which consumes 40 mW DC power (see Fig. 1.3). By proper choice of the transistor size and the length of the transmission lines, the gates of the two transistors on either sides (e.g. Q1 and Q2), experience an out-of-phase fundamental signal, and thence in-phase second harmonics would be generated at the drains of all four transistors whereas the fundamental outputs cancel each other. To improve both power efficiency and bandwidth, a passive varactor-based

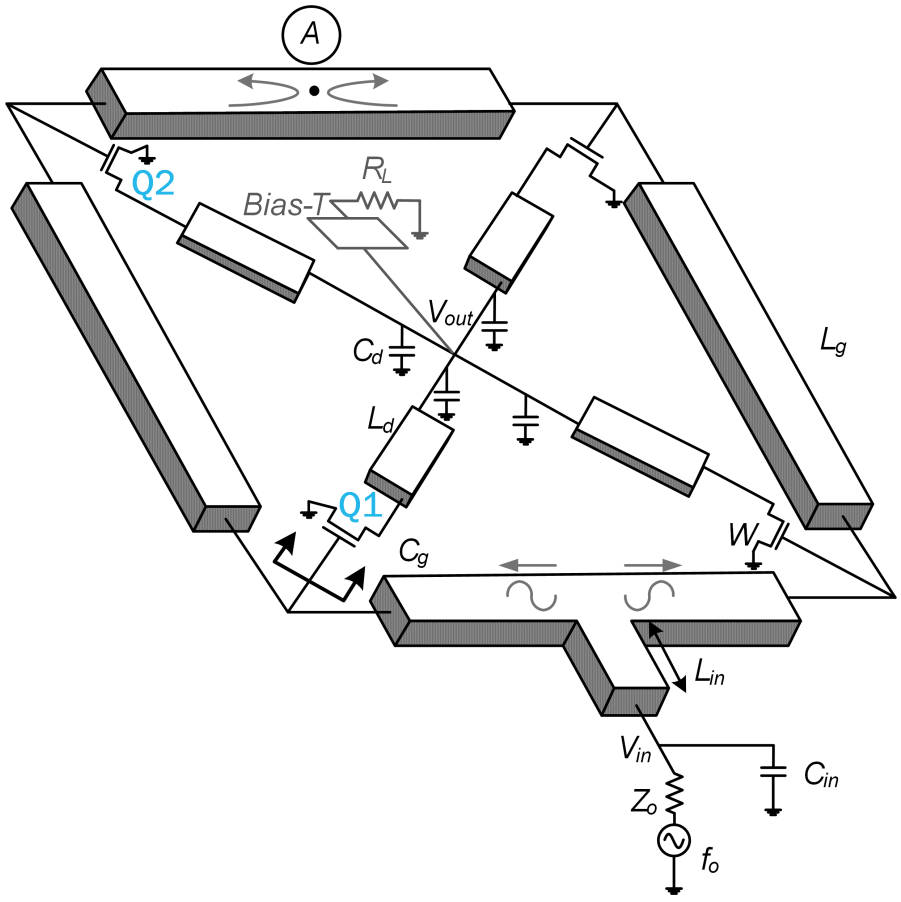

Figure 1.3: An active frequency doubler with 3 dB bandwidth of 7.8% around 243 GHz, burning 40 mW DC power in 65 nm CMOS process [2]

frequency doubler is proposed in [3]. As usual, the circuit works based on a simple symmetry which results in combining the second harmonic at the output while canceling the fundamental (see Fig. 1.4). In fact, two out-of-phase fundamental signals produce second harmonic signals which are in-phase at the output and hence added constructively

while the geometry assures that the fundamental signals cancel each other at the output. Moreover, the condition for the maximum conversion efficiency in varactors is studied in [3]. Although this frequency doubler is very wide band, still we need a wide tuning

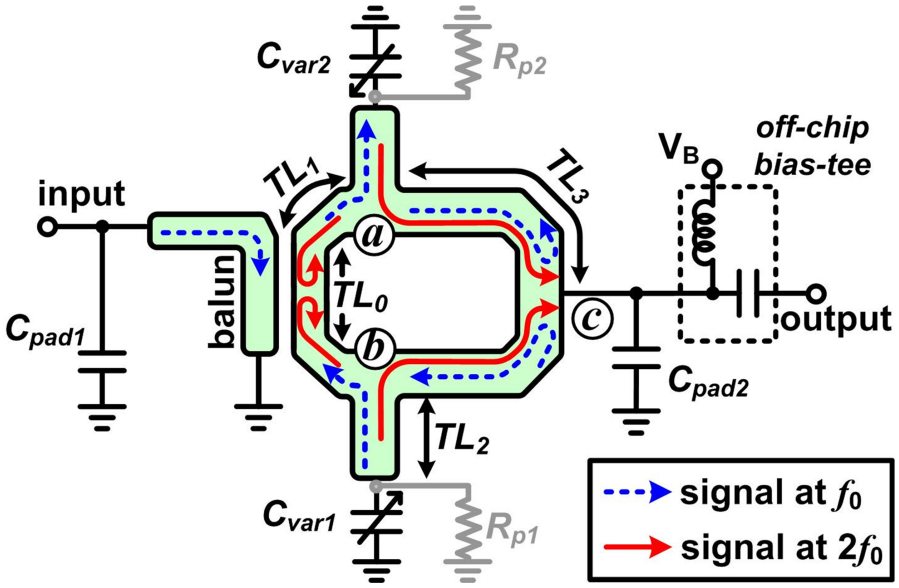

Figure 1.4: A passive frequency doubler with 3 dB bandwidth of 14.1% (simulated) around 470 GHz , burning no DC power in 65 nm CMOS process [3]

range, high output power VCO at half of the desired frequency to feed it.

1.4 Third Step: High Output Power VCO's

The most employed technique for tuning the frequency of an oscillator is to use a varactor whose capacitance can be varied by a DC voltage. In micro-wave and radio-frequency oscillators, it works properly and most of the VCO's are varactor based. However, as frequency increases, the quality factor of the varactors degrades drastically such that not only much more loss and phase noise are added to the oscillator because of them, but also they do not serve reasonably as a varying component to tune the oscilla-

tion frequency due to the loss and domination of their parasitics. In fact, introducing a varactor to an oscillator above 100 GHz, decreases the output power significantly while it is not capable of tuning the frequency as desired. To partially overcome this problem, an elegant idea is introduced in [4] which is depicted in Fig. 1.5. It is well-known that if

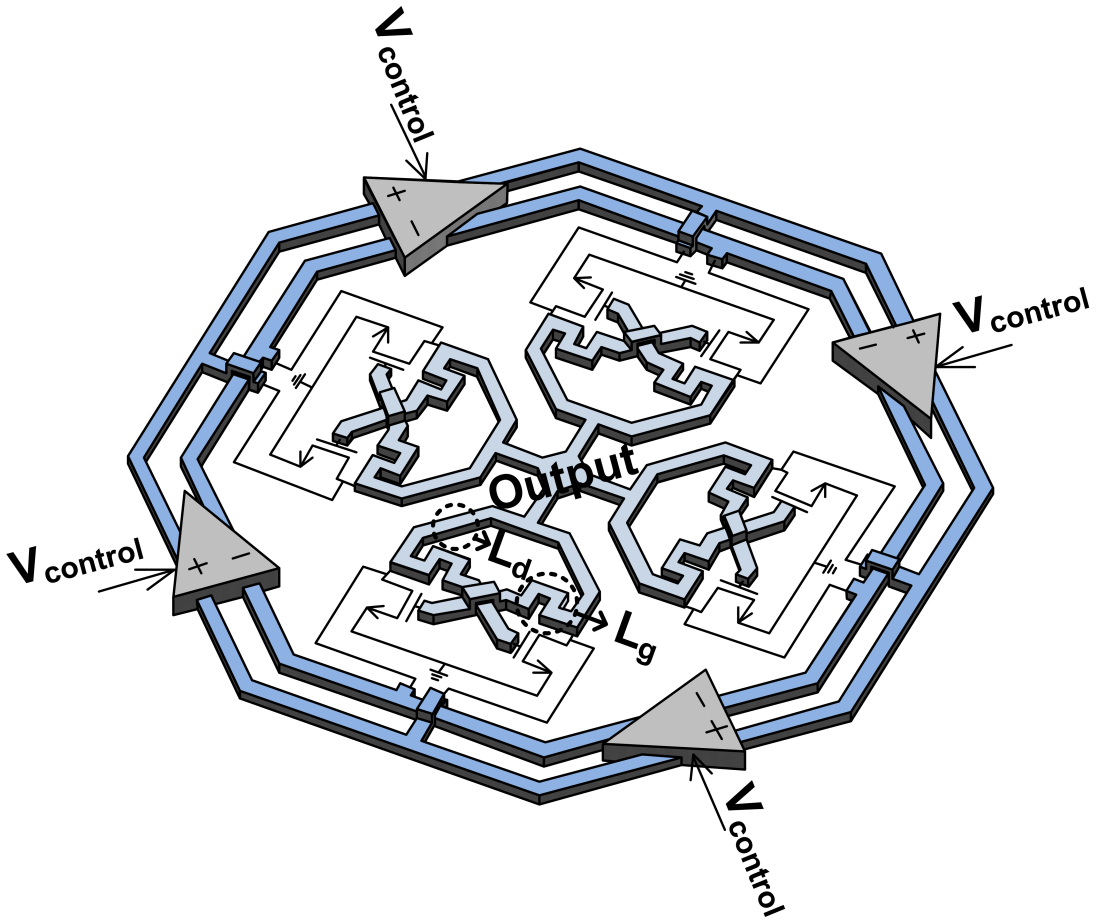

Figure 1.5: An injection locking based loop for tuning oscillation frequency without a varactor inside the oscillator block [4]

we inject enough current from one oscillator with the oscillation frequency of ω_1 to the tank of another oscillator with the oscillation frequency of ω_0 (which is close enough to ω_1), then under some mild conditions, the second oscillator will change its voltage-current phase to lock its frequency to that of the injected signal [12]. To avoid utilizing a

varactor inside an oscillator feedback loop, the injection locking is reversely employed in [4]. The frequency is changed by varying the voltage-current phase of an oscillator by the injected current of a similar oscillator. The loop guarantees a $k \times 360^\circ$ phase shift around the whole circuit and can have different stable modes which are thoroughly studied in [4]. A 290 GHz oscillator with 13 GHz tuning range (i.e. 4.5%) is reported in [4]. The loop contains four oscillators followed by four phase shifters/couplers whose phase shifts is controlled by the employed varactors. The output power of the fourth harmonic of the oscillators are added in-phase at the output node while the fundamental signal and the odd harmonics are canceled because of the symmetry in the cross-coupled structure with respect to the extraction point. In addition, the second harmonic is also canceled because of the phase shifts implied by the loop over each pair of oscillator-phase shifter/coupler. The whole structure burns 325 mW DC power while its peak output power is -1.2 dBm. The phase shifters/couplers work at fundamental frequency which is 72.5 GHz and hence the varactors are less lossy compared to 290 GHz and are capable of varying more, while they are not inside the oscillators to cause power loss.

In order to improve the output power, [5] has adopted the same method utilizing eight pairs of oscillator-phase shifter/coupler (see Fig. 1.6). The loop is constructed such that the second harmonics are combined at the output node. The varactors are used both in the oscillator block and in the phase shifters to provide enough tuning by employing two mechanisms. The interior varactors are placed in the oscillator circuits where they do not much affect the output power and therefore, they cannot tune the frequency much. However, combining the effect of these varactors with those of phase shifters results in a source with 4.3% tuning range at 256 GHz. The peak output power of this source is 4.1 dBm and the DC-to-RF efficiency of this oscillator is the best among all previously reported sources in this frequency range (1.1%). Up to this point, we had achieved mm-wave and THz sources with a reasonable tuning range and output power.

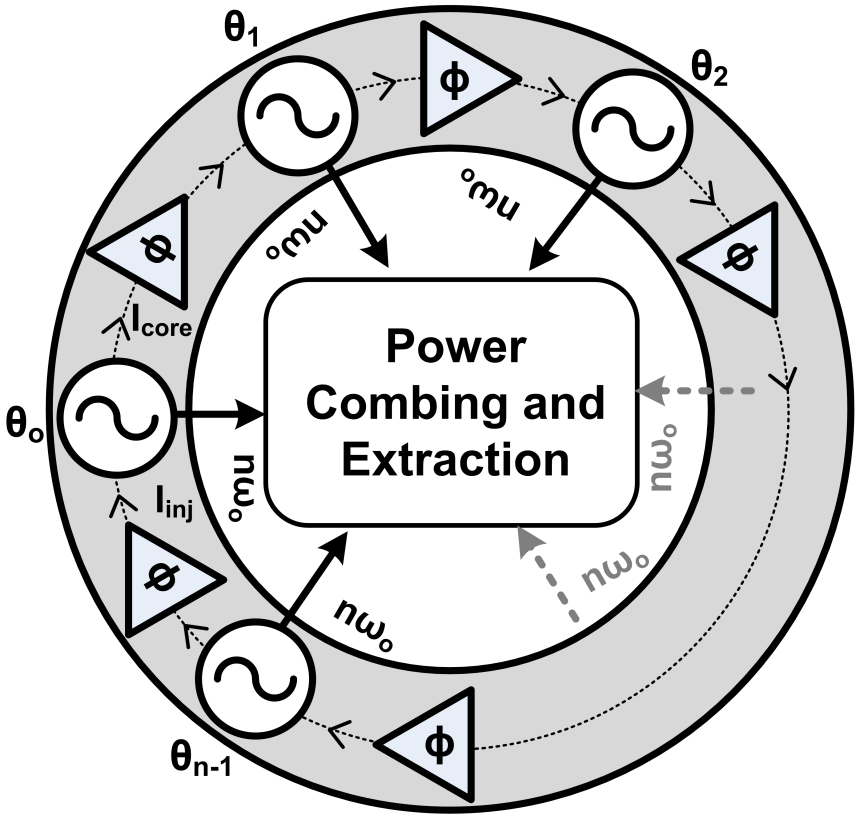

Figure 1.6: High output power tunable source at 256 GHz which uses two mechanisms in order to tune the frequency [5]

However, the DC-to-RF efficiency of none of them are enough to make CMOS/SiGe processes the proper candidates for mm-wave and THz system design. Hence, the next step is to increase the efficiency of these sources which can be done merely via a deep understanding of the device properties to become able to extract more output power while burning the same DC power.

1.5 Back to the First Step: Oscillators with High DC-to-RF efficiency and Output Power

As mentioned above, the efficiency of the previous sources are below 1.1% which limits the possibility of the future advances of mm-wave and THz systems in CMOS and SiGe processes. For instance, burning 230 mW DC power to get only 2.6 mW output power is not an acceptable result for the best mm-wave source in 2014 [5]. This emphasizes that novel techniques and different structures are required in order to increase the efficiency and it is not possible to continue the way RF oscillators are designed. New methods should replace the previous ones to extract the maximum power out of a transistor otherwise CMOS/SiGe with the state of the art f_{max} are not appropriate for mm-wave and THz system design.

A systematic approach of designing high output power and high efficiency oscillators beyond half of the f_{max} is proposed in [6]. The idea resides in the fact that the instability is a result of activity and an oscillator would be efficient if the activity of the employed transistor is preserved and is not compromised by the utilized passives which form the oscillator feedback. To design oscillators beyond the $f_{max}/2$ where the activity of the transistors are immensely degraded, [6] proposes an optimization based method where the activity figure of merit, i.e. the unilateral power gain of the network:

$$U = \frac{|y_{21} - y_{12}|^2}{4(g_{11}g_{22} - g_{12}g_{21})}, \tag{1.2}$$

is shaped and maximized at the desired frequency of oscillation while the typical model and all considered corners of the circuit are kept unstable in order to guarantee the oscillation. To shape and maximize U, two feedback mechanisms are utilized, an internal one to increase the activity of the network and to compensate the loss of the employed passives and an external feedback to shape U and also to feed part of the output power

back to the input to ensure a sustainable oscillation. The employed circuit structure is depicted in Fig. 1.7 and a 175 GHz oscillator is designed with a DC-to-RF efficiency of 11.7% and a peak output power of 4.8 dBm. The measurement results show that the oscillator maintains its high efficiency where its output power is high. Moreover, the phase noise and FoM of this oscillator are both the best among all reported CMOS/SiGe mm-wave and THz oscillators. This output power (3 mW) is extracted from a single transistor which demonstrates that a properly embedded transistor can still generate significant amount of power around 2/3 of its f_{max}. A similar structure is employed to

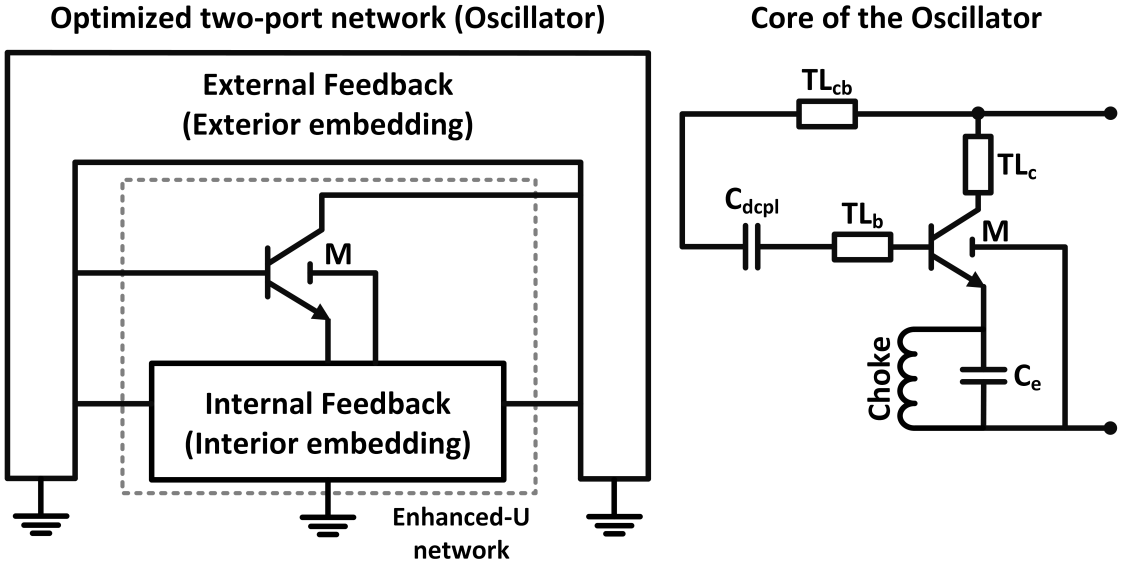

Figure 1.7: High efficiency, high output power oscillator at 175 GHz in a SiGe process with f_{max} =270 GHz [6]

design a 195 GHz VCO in a 55 nm SiGe process by optimizing the maximally efficient power gain (G_{ME}) of Eq. (1.3) in [13]. This is described in Chapter 2.

$$G_{ME} = \frac{|y_{21}|^2 - |y_{12}|^2}{4g_{11}g_{22} - 2Re(y_{12}y_{21} - 2|y_{12}|^2)} \tag{1.3}$$

Having high efficiency oscillators at frequencies beyond $f_{max}/2$ of the employed

process, we can go through the second and the third steps, to come up with efficient and tunable sources with much higher frequency and output power.

1.6 Summary and Conclusion

A decade of progress in designing mm-wave and THz sources is summarized. The highest output power, DC-to-RF efficiency, the best phase noise and FoM among all sources in mm-wave and THz frequency ranges are introduced. The journey can be continued by employing the injection-locked tuning method over the recently fabricated high efficiency oscillators. Although implementing mm-wave and THz systems in CMOS and SiGe processes are challenging, the advancements achieved at UNIC group of Cornell university during the past decade promises further progress of these systems in the low-cost processes and predicts a bright future for mm-wave and THz systems in CMOS and SiGe.

CHAPTER 2

AN EFFICIENT HIGH-POWER FUNDAMENTAL OSCILLATOR ABOVE $F_{MAX}/2$: A SYSTEMATIC DESIGN

A novel approach to design efficient high-output-power fundamental oscillators beyond $f_{max}/2$ of the employed process is presented. The idea is to shape and maximize the unilateral power gain of the network at the desired frequency using optimum passive internal and external feedback networks. The proposed technique significantly improves the output power and DC-to-RF efficiency of the oscillator. To show the feasibility of this novel approach, a 175 GHz fundamental oscillator is designed in a 130 nm SiGe BiCMOS process ($f_{max} \simeq 280$ GHz), which achieves a measured DC-to-RF efficiency of 11.7% that is markedly higher than all reported oscillators above $f_{max}/3$ of their active device. Measurements show that the designed oscillator generates a peak power of 3 mW (4.8 dBm) with a phase noise FoM of -195.4 dBc/Hz at 1 MHz offset frequency, which is the highest phase noise FoM among all reported CMOS/BiCMOS mm-wave and terahertz oscillators. The proposed method takes into account the possible PVT variations as well as modeling errors of the passive components in the design stage.

2.1 Introduction

Millimeter-waves (mm-waves) and Terahertz signals have many useful features such as non-ionizing radiation, see-through capability, and large bandwidth availability. These features make mm-waves suitable for many applications such as spectroscopy [14–16], imaging [17–19] and high data-rate communication [20–24]. In particular, the non-ionizing characteristic makes mm-waves imaging an attractive candidate for bio-medical applications [25–27]. All these systems require an efficient mm-wave signal source that generates adequate power. Because of the rising demand in mm-wave applications,

signal generation in this frequency range, especially in low-cost processes such as SiGe and CMOS has recently become a trend [1, 5, 28–33].

Several mm-wave oscillators in SiGe and CMOS processes have been recently reported [1, 4, 5, 28–32, 34–40]. Two challenging characteristics of a mm-wave source are output power and DC-to-RF efficiency. This is due to the low efficiency of active devices close to their maximum frequency of oscillation (f_{max}) as well as the high loss of the passive components at these frequencies. Since signal generation is not efficient close to f_{max} and moreover, fundamental signal cannot be generated above f_{max}, harmonic extraction and frequency multipliers have been exploited to further increase the frequency of the signal sources [5, 31, 33, 40–43]. To achieve a higher output power and efficiency in these oscillators, generating efficient fundamental power is targeted [2, 40].

There has been a long-lasting research to maximize the output power of high-frequency oscillators [44–53]. In these works, in a traditional circuit topology, the passive component values are selected to maximize the generated power. In an alternative technique, the target is to increase the added power (the difference between the real power flowing into the device and out of it) by designing an optimum passive embedding. This approach is rigorously explained in [10] and has been employed in [1, 5, 11, 40]. In fact, instead of the added power, a mixed function of the added power and the electrical variables (e.g., input/output voltages) are optimized in these works. Therefore, it does not guarantee the maximum net output power. This stems from the fact that it is not possible to formulate the added power of a two-port network using only the circuit parameters (i.e., independent of the electrical variables such as input/output voltages) [11]. Moreover, there is no systematic way to push the circuit towards the desired optimum condition.

Oscillation is a result of instability and the activity is a necessary condition for the

instability. The activity of a device usually degrades as the frequency increases. Meanwhile, the ability of a network for power generation decreases as its activity degrades and vanishes at the f_{max} [8, 10]. The measure of activity of a two-port network is its unilateral power gain (U) which is proved to be invariant for a two-port network under any four-port linear-lossless-reciprocal (FPLLR) embedding [8, 54]. However, it is shown in this work that since an integrated transistor is not a two-port network, using FPLLR embeddings, it is possible to increase the activity of the two-port network composed of that transistor (and hence to improve U).

In this paper, a novel approach to design efficient fundamental oscillators close to f_{max} is introduced. The proposed method shapes the unilateral power gain of the network to have a peak at the desired frequency of oscillation. The network then naturally selects the peak frequency as its oscillation frequency. To the best of our knowledge, this is the first time that the oscillation frequency is selected by forming a local maximum in the U at the desired frequency. The high efficiency of the designed oscillator is a result of forming a local maximum for the device activity at the desired frequency of oscillation. Burning the same DC power, the enhanced activity results in higher output power generation and thence a better DC-to-RF efficiency.

Using this technique, a fundamental oscillator close to 2/3 of f_{max} is designed in a 130 nm SiGe process (with f_{max} $\simeq$280 GHz [55]). The measurements show that this oscillator achieves the highest output power (4.8 dBm) and DC-to-RF efficiency (11.7%) among all oscillators working above $f_{max}/3$. Moreover, it achieves the best phase noise FoM (-195.4 dBc/Hz at 1 MHz offset frequency) among all mm-wave sources in CMOS/SiGe processes.

The rest of the paper is organized as follows. In Section 2.2 the concepts of device activity and stability are reviewed. Section 2.3 shows how the activity of a two-port net-

Figure 2.1: A two-port network

work composed of a transistor can be improved. The proposed method for designing a high efficiency oscillator is described in Section 2.4. A design example is demonstrated in Section 2.5. The measurement results are reported in Section 2.6 and finally, Section 2.7 concludes this work.

2.2 Basic Properties of a Two-Port Network

In this section, we review the properties of two-port networks that enable us to design an efficient oscillator. First, the activity and stability of these networks are reviewed and then the unilateral power gain (Mason's invariant) is discussed.

2.2.1 Activity and Stability

A two-port network shown in Fig. 2.1, can be represented by its admittance parameters,

$$\begin{aligned} I_1 &= y_{11}V_1 + y_{12}V_2 \\ I_2 &= y_{21}V_1 + y_{22}V_2, \end{aligned} \tag{2.1}$$

while $I_1 = I_1'$ and $I_2 = I_2'$ [56]. These equations constitute a complete small-signal description of a two-port network at a given bias point and frequency.

The network is *active* at a frequency if the total real signal power flowing into the network is negative at that frequency [10]. Hence, a two-port network is capable of power amplification or oscillation only if it is active [10]. Using Eq. (2.1), the complex signal power flowing into the network can be expressed as:

$$P = P_R + jP_I = V_1 I_1^* + V_2 I_2^* = y_{11}^* |V_1|^2 + y_{22}^* |V_2|^2 + y_{12}^* V_1 V_2^* + y_{21}^* V_1^* V_2,$$

where P_R and P_I are real numbers and $-P_R$ is the added power which is desired to be maximized. It is straightforward to show that:

$$\frac{P_R}{|V_1||V_2|} = a^{-1} g_{11} + a g_{22} + |y_{12} + y_{21}^*| \cos(\measuredangle(y_{12} + y_{21}^*) + \alpha), \tag{2.2}$$

where

$$a = |\frac{V_2}{V_1}|, \quad \alpha = \measuredangle \frac{V_2}{V_1},$$

$g_{11} = \mathrm{Re}(y_{11}^*)$ and $g_{22} = \mathrm{Re}(y_{22}^*)$. Obviously, the sign of the left hand side of (2.2) is set by P_R whose negative sign means activity. If either $g_{11} < 0$ or $g_{22} < 0$, then P_R can be made negative by making the positive real quantity "a" sufficiently small or large, respectively. This kind of activity is often called *negative-conductance activity* [10]. However, in most practical cases, g_{11} and g_{22} are both positive. In this case, it can be shown that:

$$\min(\frac{P_R}{|V_1||V_2|}) = 2\sqrt{g_{11} g_{22}} - |y_{12} + y_{21}^*|, \tag{2.3}$$

which happens when

$$a = \sqrt{g_{11}/g_{22}}$$

and

$$\alpha = (2k+1)\pi - \measuredangle(y_{12} + y_{21}^*).$$

Thus, P_R can be made negative and the network is active if

$$4g_{11}g_{22} < |y_{21} + y_{12}^*|^2.$$

This kind of activity is called *transfer activity* [10] since it depends on both forward and reverse transfer parameters (i.e. both y_{21} and y_{12}) of the network. In summary, a two-port network is active if at least one of the following inequalities is satisfied:

$$g_{11} < 0, \tag{2.4}$$

$$g_{22} < 0, \tag{2.5}$$

$$4g_{11}g_{22} < |y_{21} + y_{12}^*|^2. \tag{2.6}$$

It should be emphasized that these conditions are bias and frequency dependent since the y-parameters vary with bias and operation frequency.

Remark: The optimum case of Eq. (2.3) coincides with the maximum added power only if $|V_1|$ and $|V_2|$ are independent of the y-parameters.

Activity of a device can potentially lead to instability which means uncontrolled increase of the amplitude of network voltages or currents in the absence of any driving source [56]. A two-port network is unconditionally stable at a desired frequency if it remains stable for all passive terminations at its input and output ports [57]. It can be shown that a two-port network is stable for all possible passive terminations if the following conditions are simultaneously satisfied [10]:

$$g_{11} \geq 0, \tag{2.7}$$

$$g_{22} \geq 0, \tag{2.8}$$

$$2g_{11}g_{22} - M \geq L, \tag{2.9}$$

where

$$M + jN = y_{12}y_{21} \text{ and } L = \sqrt{M^2 + N^2}. \tag{2.10}$$

The first two inequalities are satisfied for most active devices and hence any potential instability of a transistor is usually caused by the failure to satisfy the third inequality (2.9).

Remark: By comparing the inequalities defining activity with those of stability, it is clear that if a network is not active, it cannot be unstable. In other words, activity is a necessary (but not sufficient) condition for instability.

2.2.2 Unilateral Power Gain

The unilateral power gain (U) a.k.a. ***Mason's invariant*** represents the transfer activity of a two-port network and hence it can be derived from Eq. (2.6). Subtracting $4g_{12}g_{21}$ from both sides of (2.6) results in a new condition for transfer activity as:

$$4(g_{11}g_{22} - g_{12}g_{21}) < |y_{21} - y_{12}|^2. \tag{2.11}$$

Dividing both sides of (2.11) by its left side results in the so-called Mason's invariant U:

$$U = \frac{|y_{21} - y_{12}|^2}{4(g_{11}g_{22} - g_{12}g_{21})}, \tag{2.12}$$

which is a real number that depends on bias and frequency.

Comparing (2.6) and (2.12), we can see that if $U > 1$ (or $U < 0$), the network has transfer activity.

Normally, U decreases as frequency increases and above $f_{max}/2$ it drops by a slope of 20 dB/dec and becomes unity at $f = f_{max}$. Beyond the f_{max}, the device is not active anymore and hence, not capable of power amplification or oscillation in any configuration.

Mason's invariant U has several useful properties including:

I. It is invariant under any FPLLR embedding. This means connecting lossless components such as capacitors, inductors, transformers and transmission lines between any nodes of a two-port network does not change its U. This property is vital for an appropriate measure of activity which is not expected to be changed by a lossless-reciprocal embedding.

II. U of a three-terminal device (i.e. a two-port network such as a discreet transistor) is invariant to any permutation of its terminals. This property in fact can be seen as a particular case of the previous one, where the embedding is composed of a collection of lossless wires which permute the terminals. This special characteristic of U allows us to define U of a transistor independent of its configuration, e.g., common-emitter, -collector or -base, which is essential for a measure of activity.

III. The power gain of a unilateral two-port network, (i.e. $y_{12} = 0$), which is conjugately matched at both ports, is equal to U [8, 54]. That is why U is called the "unilateral power gain" of the two-port network.

2.3 Variant Mason's Invariant

In this section, it is shown that in contrary to common belief, for an integrated transistor, the unilateral power gain or the so-called Mason's invariant (U) of the network, can be changed with an FPLLR embedding. By using an internal degeneration capacitor, not only U can be increased but also it can be made infinite at some frequencies. This phenomenon has been long overlooked since U was initially proposed as a figure of merit for discreet transistors which have only three terminals [8].

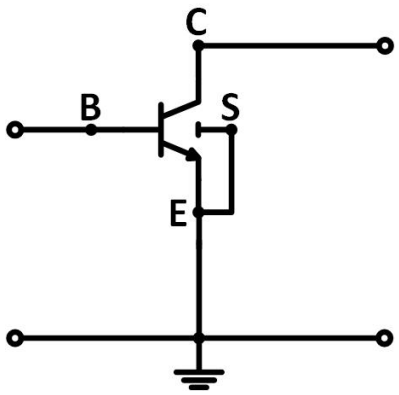

Figure 2.2: An integrated transistor used in a two-port network configuration

Remark: Mason's theorem proves the invariance of U only for a two-port network under any FPLLR embedding. Hence, a lossy embedding is capable of changing U. See [58] to find how a lossy embedding not only can change U, but also can increase it. (Please notice that unboundedness proof of [58] is not completely correct.)

It should be emphasized that the result of this section does not contradict Mason's theory of the invariance. In fact, U is *only* defined for a two-port network and its invariance is then proved *only* for a two-port network. An integrated transistor is a three-port network that we usually use it in a two-port configuration and therefore we can define U as a measure of its activity. For instance, Fig. 2.2 demonstrates an integrated BJT which is used as a two-port network by connecting its bulk and emitter together.

To the best of our knowledge, the ability of changing the U of a network composed of an integrated transistor with an FPLLR embedding has never been reported or mentioned in the literature before and therefor, it is thoroughly studied in this section.

In this work, we study the ability of making a new two-port network composed of an integrated transistor such that the resulting network has higher U compared to that of the two-port network of Fig. 2.2. An integrated transistor is demonstrated in Fig. 2.3

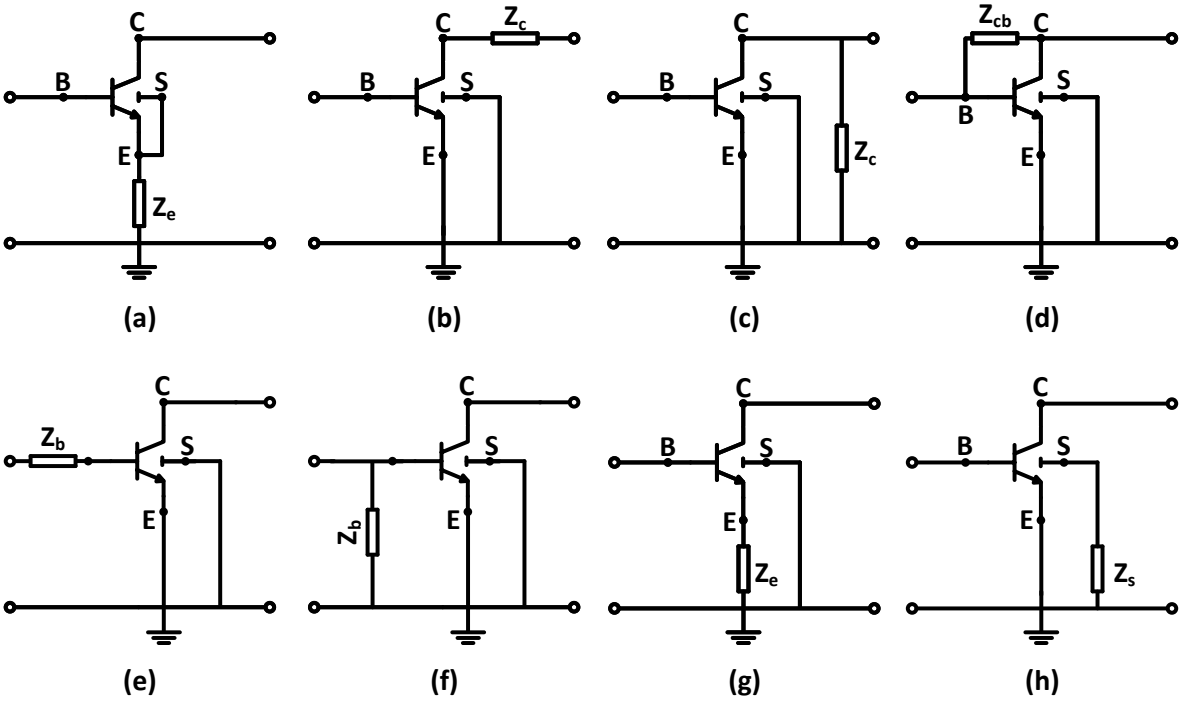

Figure 2.3: The LLR extra components might have different effects on U: (a)-Z_e is in series with the whole transistor network (b)-Z_c is in series with the whole transistor network (c)-Z_{cc} is in parallel with the whole transistor network (d)-Z_{cb} is in parallel with the whole transistor network (e)-Z_b is in series with the whole transistor network (f)-Z_{bb} is in parallel with the whole transistor network (g)-Z_e is an internal component of the two-port network (h)-Z_s is an internal component of the two-port network

along with an LLR component. In Figs. 2.3-(a)-(f) the extra LLR component serves as an embedding to the two-port network of Fig. 2.2, which according to [8] does not change the unilateral power gain of the resultant network compared to that of Fig. 2.2. However, in Figs. 2.3-(g) and -(h), the LLR component is placed inside the device and therefore U of the new two-port network, is different from that of the transistor itself in Fig. 2.2. Although a lossless Z_s in Fig. 2.3-(h) can change U, this is not studied here since it is not a practical case.

As can be seen from Fig. 2.3, the role of the extra component would not change if the BJT is replaced by a CMOS transistor or any other device with four nodes. Hence, the results hold for both BJT and CMOS transistors.

Remark: It is worthwhile mentioning that having the y-parameters of the extra LLR components in Fig. 2.3 and those of the transistor in Fig. 2.2, it is possible to derive the y-parameters of the new two-port networks of Figs. 2.3 (a) to (f) using circuit theory. However, the y-parameters of Figs. 2.3 (g) and (h) cannot be derived using the circuit theory. Combined with the proof of invariance in [8], this fact indicates that the unilateral power gain of a transistor in Figs. 2.3 (g) and (h) is not preserved. Please note that the structure of Fig. 2.2 can be recognized in Figs. 2.3 (a) to (f) whereas Figs. 2.3 (g) and (h) do not contain such a network.

In the sequel we study a lumped model of an integrated transistor along with two PDK transistor models from two different processes to show how an LLR degeneration impedance (Fig. **??** (g)) affects Mason's invariant of the resulting network.

2.3.1 Lumped Model

A single simulation which shows that an LLR Z_e in Fig. 2.3 (g) changes the U is sufficient to prove that U is not invariant for this structure. However, to show the generality, this effect is studied using the hybrid-π model of an integrated transistor.

A hybrid-π model of a BJT is depicted in Fig. 2.4. Comprehensive study of this model indicates that:

- Omitting either of r_c or C_b results in a U which is independent of degeneration impedance in Fig. 2.3 (g). This is clear from Mason's theorem since when r_c is

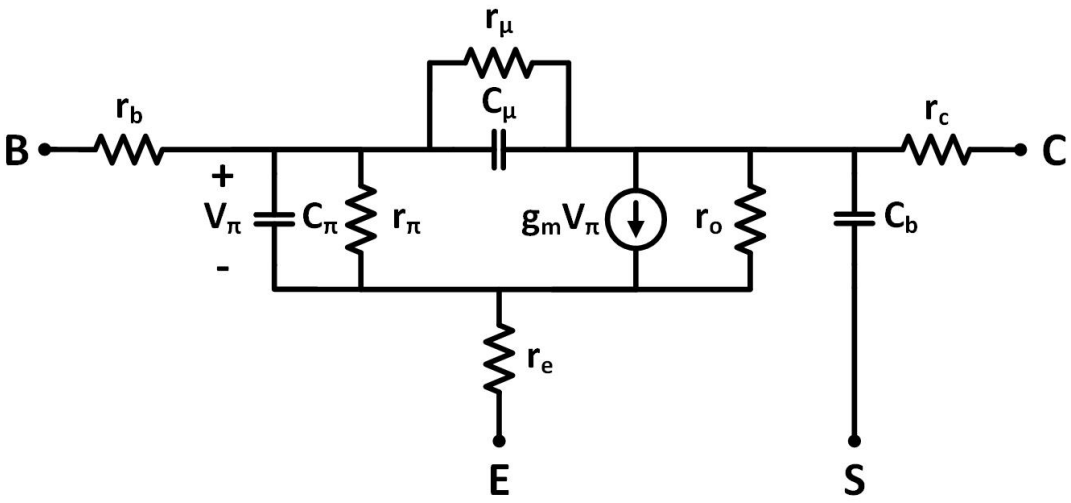

Figure 2.4: Hybrid-π model of a BJT

omitted, C_b is an LLR embedding at the output and hence does not affect U. If C_b is omitted, then the network becomes a two-port one and hence its U will be preserved under any FPLLR embedding.

- r_μ and c_μ have the worst effect on degradation of U. Without them U is mostly related to r_π and increases enormously as r_π decreases.
- r_b and r_e degrade U but not as much as r_μ. The effect of r_b and r_e is more visible at high frequencies.
- Large r_o in addition to capacitive degeneration results in negative and infinite U at some frequencies.
- When all r_b, r_e, r_μ and r_o are considered, U of the hybrid-π model does not become infinite at any frequency. However, the PDK models always have frequencies where U becomes infinite.
- Degeneration capacitor, C_e can increase U at some frequencies and decrease it at others (changing the slope). For instance in some cases it is possible to increase

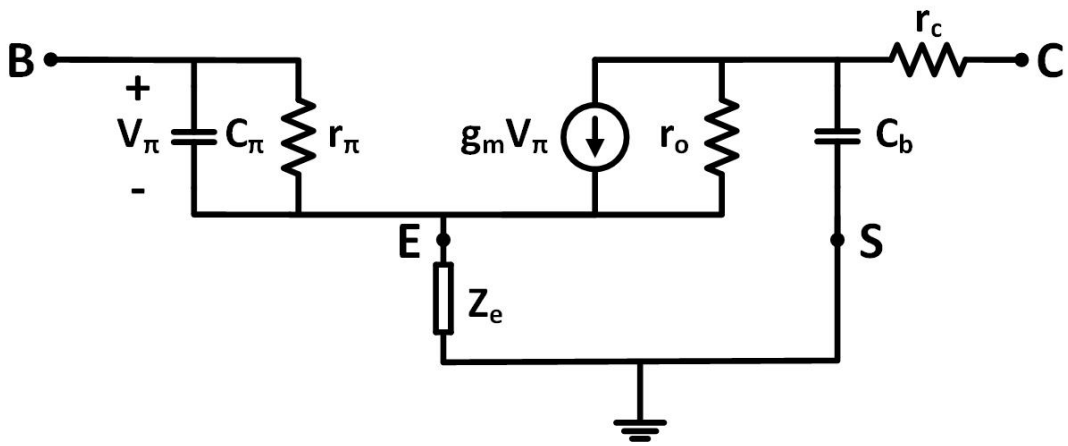

Figure 2.5: Simplified model of a BJT along with the added LLR component (Z_e) in series with the emitter terminal. The following values are assumed for simulations: $r_\pi = 500\Omega$, $C_\pi = 25fF$, $C_b = 10fF$, $r_o = 2k\Omega$, $r_c = 3\Omega$ and $g_m = 20m\mho$.

U at $f_{max}/2$ while f_{max} itself does not change much or decreases.

- It is interesting that r_c alone degrades U but together with C_e, U can be improved.

For simplicity, assume that $r_\mu = \infty$, $C_\mu = 0$ and $r_b = r_e = 0$ (which results in high f_{max}). The simplified model along with the degeneration component are shown in Fig. 2.5. In order to study the effect of the internal degeneration on the U, the y-parameters of the two-port network of Fig. 2.5 are derived:

$$
\begin{aligned}
y_{11} &= \frac{y_e(y_b + y_c + y_o) + y_o(y_b + y_c)}{(y_e + y_\pi + g_m)(y_b + y_c + y_o) + y_o(y_b + y_c) - g_m y_o} y_\pi \\
y_{12} &= \frac{-y_c y_o}{(g_m + y_o)(y_b + y_c) + (y_e + y_\pi)(y_b + y_c + y_o)} y_\pi \\
y_{21} &= \frac{y_e y_c (g_m y_e - y_o y_\pi)}{(y_e + y_\pi)(y_e y_o + (y_b + y_c)(y_o + y_e)) + (y_b + y_c)(g_m y_e - y_o y_\pi)} y_o \\
y_{22} &= \frac{(y_b(y_e + y_\pi + y_o + g_m) + y_o(y_e + y_\pi))}{(y_c + y_b)(y_e + y_\pi + y_o + g_m) + y_o(y_e + y_\pi)} y_c,
\end{aligned}
$$

where $y_o = 1/r_o$, $y_c = 1/r_c$, $y_b = j\omega C_b$, $y_e = 1/Z_e$ and $y_\pi = j\omega C_\pi + 1/r_\pi$. Having the y-parameters, U can be calculated from Eq. (2.12).

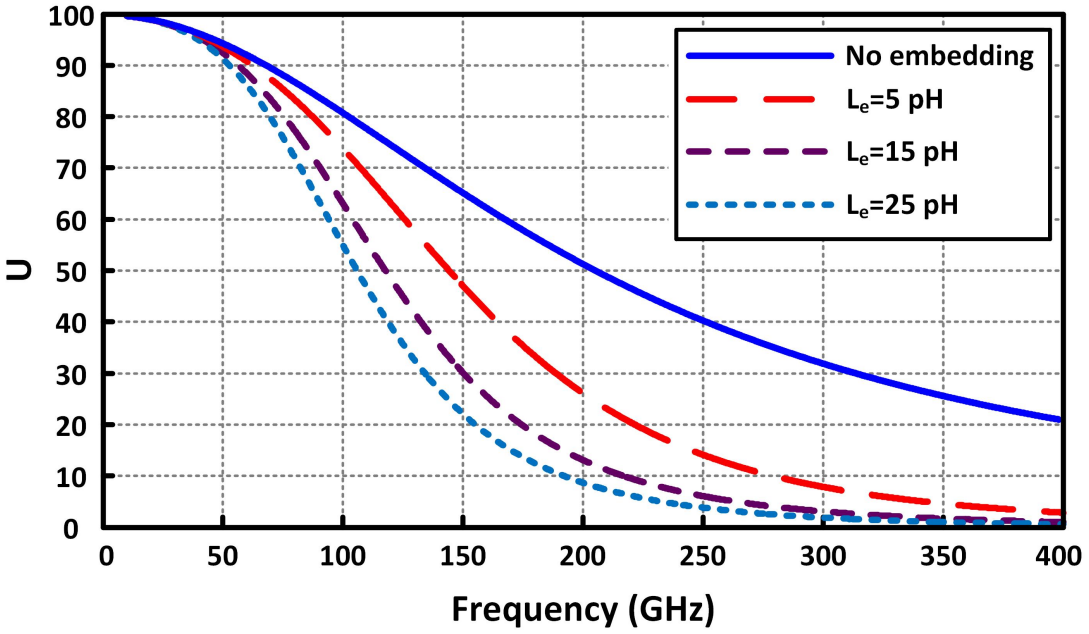

Figure 2.6: U vs. Frequency for the simplified model of Fig. 2.5 for several values of L_e ($Z_e = j\omega L_e$)

As the first case, Z_e is replaced by an inductor. Fig. 2.6 demonstrates how this affects the unilateral power gain of the lumped model of Fig. 2.5. It shows that such an FPLLR embedding degrades U at all frequencies and hence decreases f_{max}.

Next, Z_e is replaced by a capacitor. Fig. 2.7 demonstrates how C_e changes the unilateral power gain of whole two-port network with respect to that of the transistor alone. It is obvious that U becomes unbounded at a frequency (f_{pi}) which is a function of C_e. The effect of C_e on U vanishes as C_e becomes very large since $Z_e = 1/j\omega C_e$ diminishes as C_e increases.

The above examples prove that Mason's invariant U can be changed for an integrated transistor by an FPLLR embedding.

Furthermore, having a capacitor in the emitter results in a negative input resistance

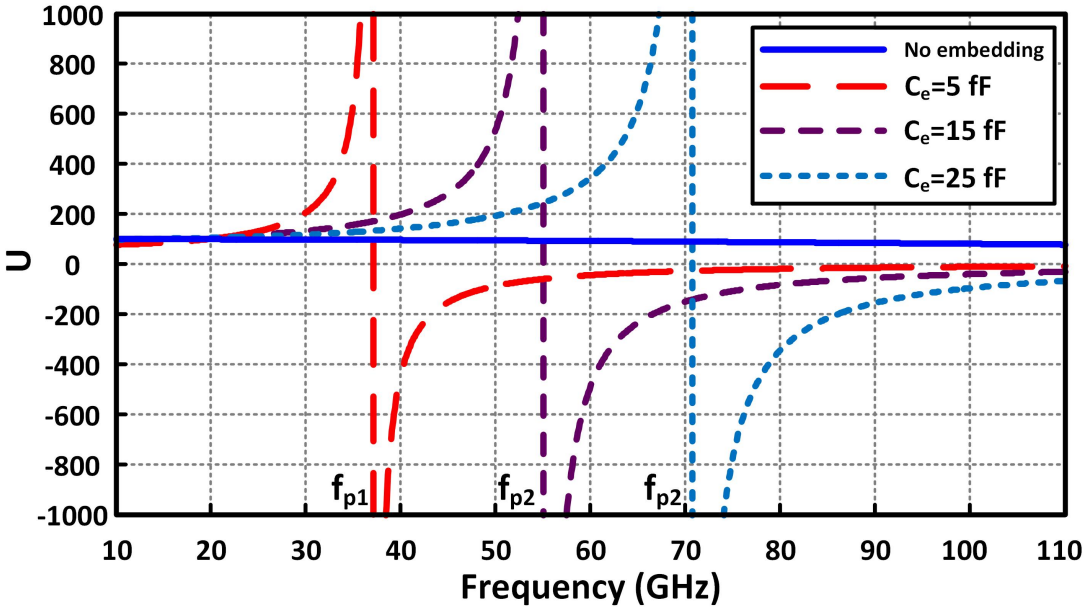

Figure 2.7: U vs. Frequency for the simplified model of Fig. 2.5 for several values of C_e ($Z_e = 1/j\omega C_e$)

looking into the base. Figure 2.8 shows that $g_{11} < 0$ for a large frequency interval while $g_{22} > 0$. Consequently, the resulting two-port network has both negative conductance and transfer activity. According to the unilateralization theorem [8], there exists an FPLLR embedding which results in a new two-port network with positive g_{11} and g_{22} and with no changes in U.

2.3.2 PDK Model

To show that the supplementary capacitor affects a real transistor similarly, an HBT model from STMicroelectronics 130 nm SiGe process is employed. The selected transistor has a 2×4.5 μm emitter length and is simply biased by a 10 μA current source injected into its base while the supply voltage is 1.6 V. Fig. 2.9 illustrates U versus

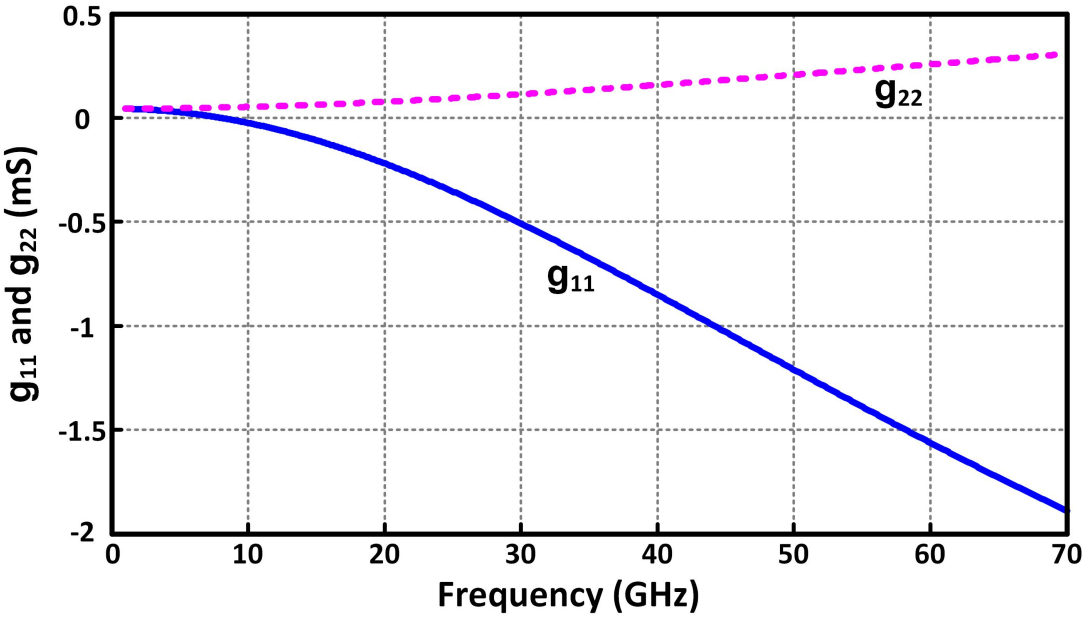

Figure 2.8: g_{11} and g_{22} vs. Frequency for the simplified model of Fig. 2.5 with $C_e = 10$ fF ($Z_e = 1/j\omega C_e$)

frequency for this transistor. Fig. 2.10 demonstrates U versus frequency for different values of C_e. Fig. 2.11 depicts g_{11} and g_{22} vs. frequency. Analogous to the previous case, g_{11} is almost negative at all frequencies and g_{22} is positive everywhere. Fig. 2.12 reveals a remarkable point about the real transistor model compared to the simplified model of Fig. 2.5. For the selected PDK transistor, U has two distinct poles, one close to 6 $GHz = f_{p1}$ and the other one around 60 $GHz = f_{p2}$ where it becomes unbounded, whereas for the simplified model U becomes unbounded only at one frequency. Additionally, Fig. 2.12 shows that U is negative between f_{p1} and f_{p2} which means that the two-port network is active in this interval. However, the unilateralization theorem [8] does not provide any information about the possible transformations using FPLLR embeddings and hence this case needs to be further studied in future. To show that the proposed embedding can improve U in reality, it is assumed that C_e has a finite quality factor. Fig. 2.13 shows U versus frequency for different values of C_e with a quality

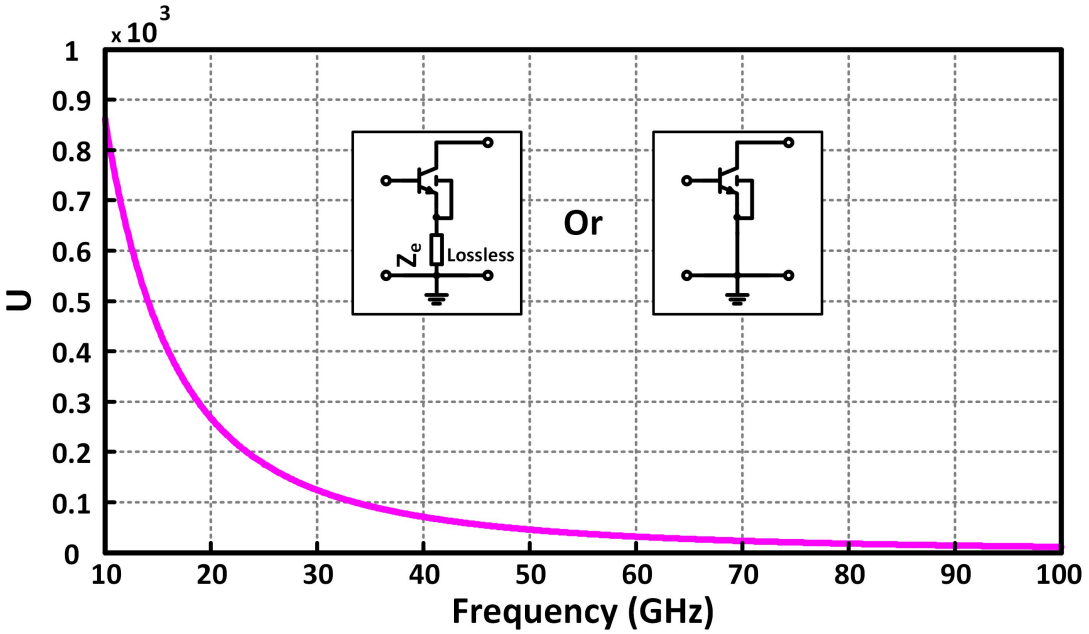

Figure 2.9: Simulated U vs. Frequency for a real transistor from a 130 nm SiGe process with no embedding

factor of 15. Compared to Fig. 2.10, where the capacitor is ideal (i.e. $Q = \infty$), f_p is decreased for each C_e but the same overal behavior is observed. This confirms the feasibility of the proposed embedding in the actual circuits. To show that the same effect can be seen in other processes, the LLR degeneration is studied on an HBT transistor (2×5 μm emitter length) from 55 nm STMicroelectronics process and also on a CMOS transistor (width of 10×1 μm) of a 130 nm SiGe process (Figs. 2.14 and 2.15). It is obvious that the capacitive degeneration increases both f_{max} and the slope of U vs. frequency for both transistors. A transistor with enhanced U can be exploited in several ways. First, since U and the power gain are tightly related [10], it can be used to design amplifiers with higher power gain. Second, since generating more power with a two-port network is closely coupled to its U [10], it can be employed to design oscillators with higher output power. The importance of boosting U becomes more substantial at frequencies close to f_{max}, where U is naturally small. Thus, both amplifiers and oscillators benefit

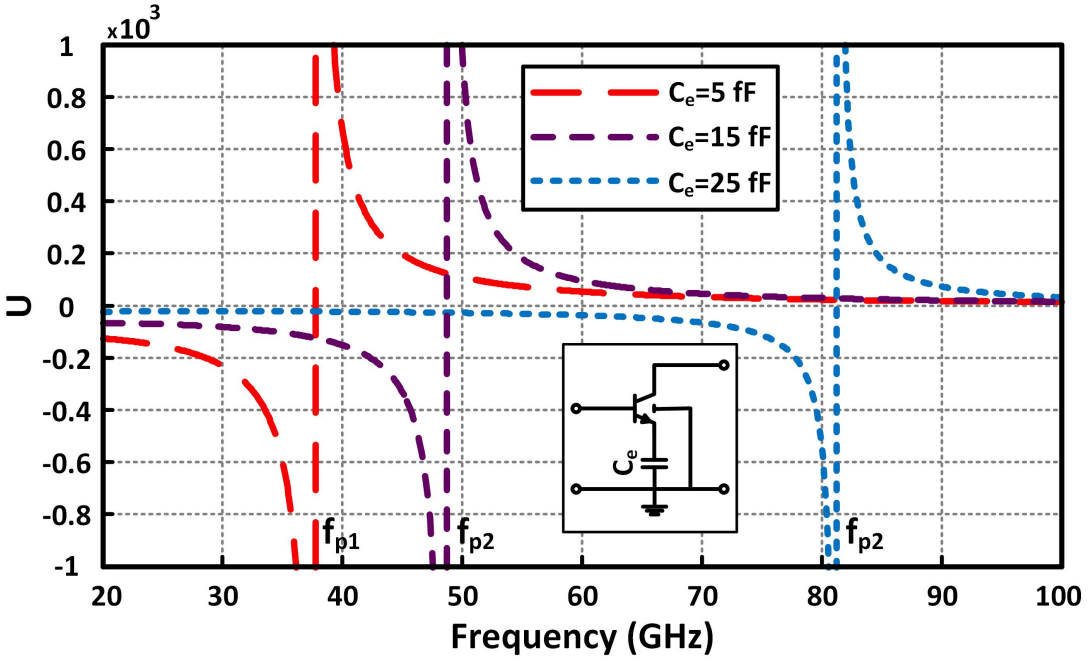

Figure 2.10: Simulated U vs. Frequency for different capacitances, for the selected transistor from a 130 nm SiGe process

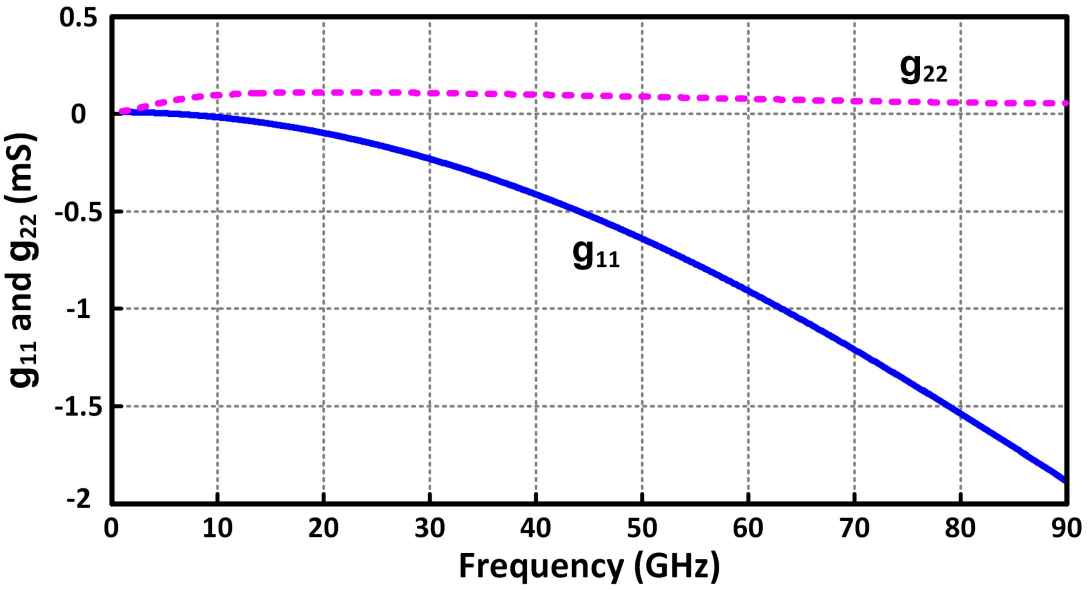

Figure 2.11: Simulated g_{11} and g_{22} of the real transistor from 130 nm SiGe process with C_e = 10 fF

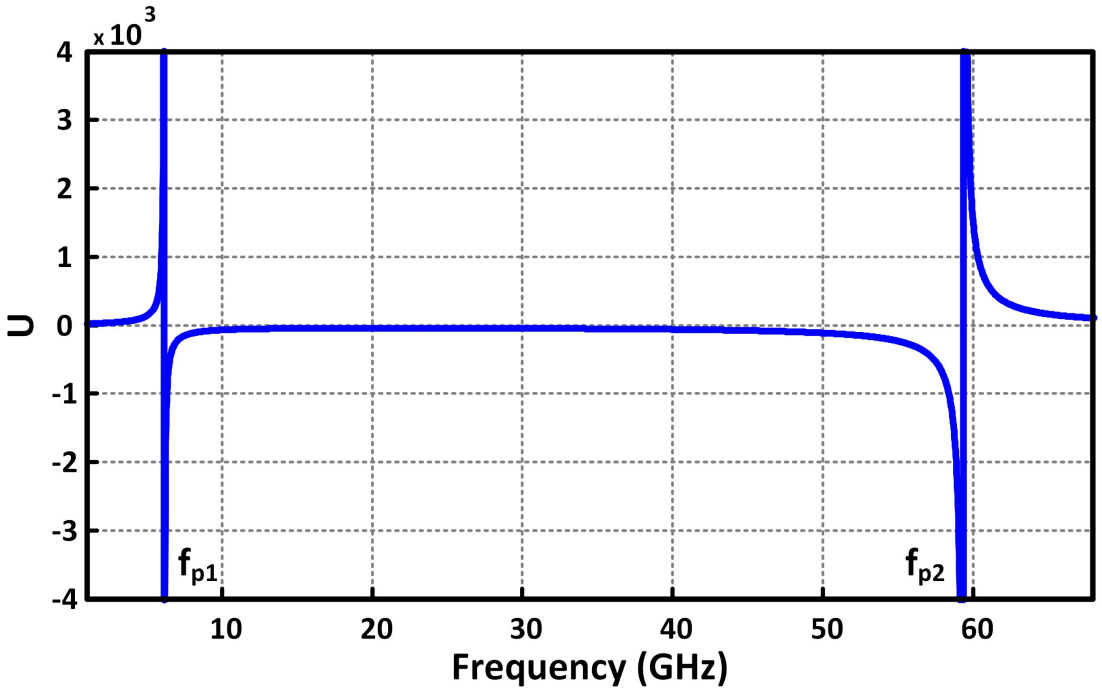

Figure 2.12: Simulated U of the real transistor from 130 nm SiGe process vs. frequency with $C_e = 10fF$.

more from an enhanced U at higher frequencies. Third, the proposed embedding can be delicately utilized to fabricate better transistors, i.e. with higher f_{max}. It is well-known that beyond $f_{max}/2$, U decreases approximately by a constant slope of 20 dB/dec. Therefore, if at a desired frequency above $f_{max}/2$, U is increased for instance, by 3 dB, it is "as if" we have a device whose f_{max} is enhanced by 41% compared to the original transistor.

2.4 Proposed Structure of the Oscillator

In this section, a new method for designing efficient high-power fundamental oscillators above $f_{max}/2$ of the active device is introduced. The basic concept is depicted in Fig. 2.16. Two co-designed linear reciprocal embeddings are exploited to achieve an efficient

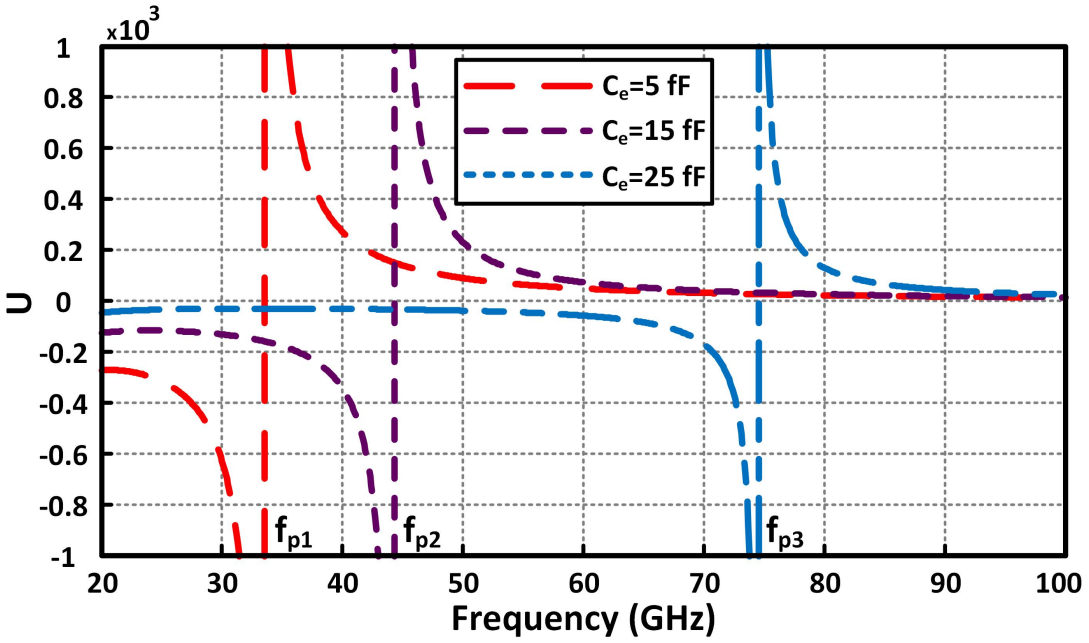

Figure 2.13: Simulated U vs. Frequency for different values of C_e with quality factor Q=15, for a real transistor from a 130 nm SiGe process

oscillator: a capacitive internal feedback and an inductive external feedback. The circuit implementation of this concept is demonstrated in Fig. 2.17.

2.4.1 Internal Feedback

An internal emitter/source degeneration of Fig. 2.3-(g), serves as an interior part of the integrated transistor that is completely studied in the previous section. In addition to increasing U, the internal capacitive degeneration, forms a positive feedback which destabilizes the network and results in negative real part of the input admittance as shown in Fig. 2.11. It is noteworthy that the instability caused by this capacitive feedback is a negative conductance instability (i.e. inequalities (2.7) and/or (2.8) are violated) and is not a source of sustainable oscillation in this circuit. To guarantee a stable oscillation,

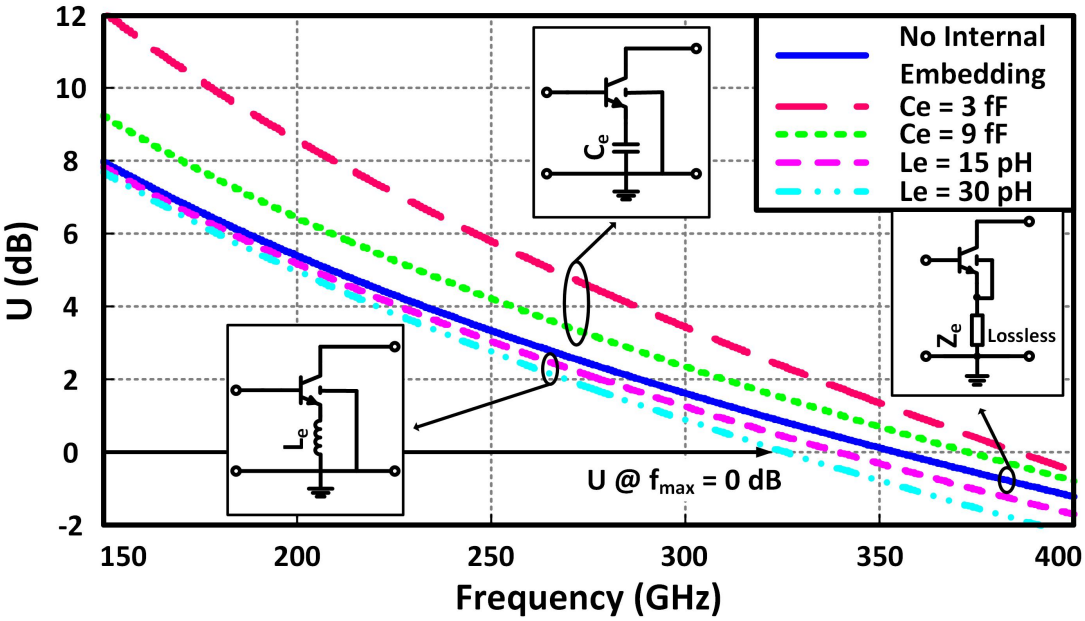

Figure 2.14: Simulated U for different emitter degenerations for an HBT with 2×5 μm emitter length from a 55 nm SiGe process.

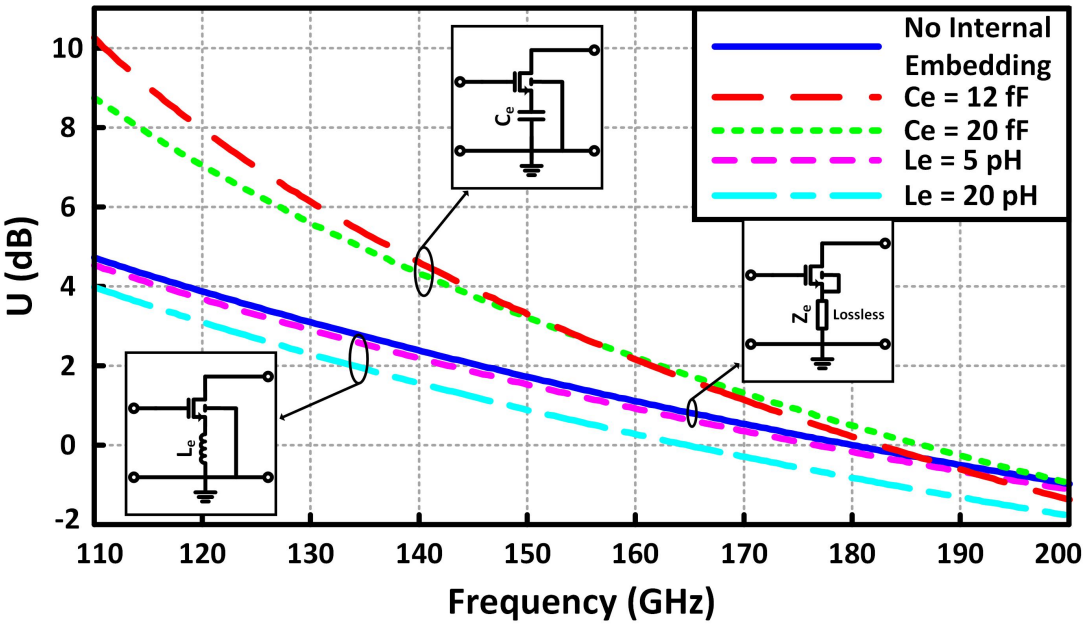

Figure 2.15: Simulated U for different source degenerations for a CMOS with 10×1 μm width from a 130 nm SiGe process.

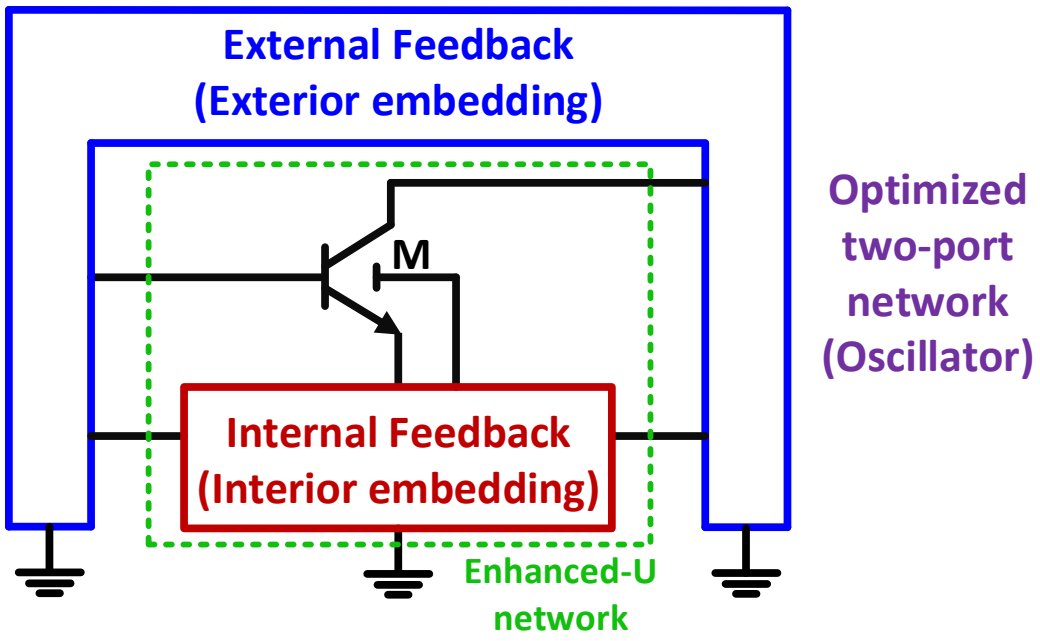

Figure 2.16: The basic concept of the proposed method to design an efficient oscillator beyond $f_{max}/2$

this feedback has to be co-designed with the external one, otherwise the transistor might not be able to feed part of its output power back to its input to sustain the oscillation.

2.4.2 External Feedback

Self-sustained oscillation can be guaranteed by an external feedback which is capable of making *transfer-instability* by violating the inequality (2.9). In contrary to the internal feedback, the external one does not change U [8]. In reality, since the employed passive components are lossy, this embedding usually decreases U.

The external inductive embedding, serves as a positive feedback whose role is two-folded:

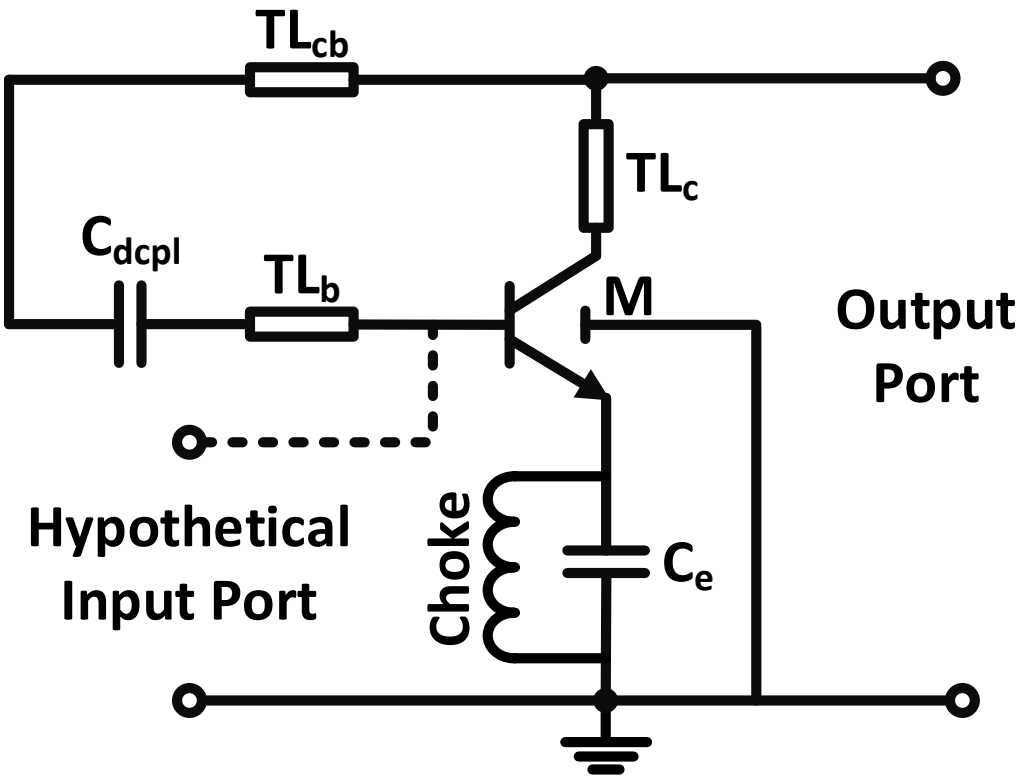

Figure 2.17: Oscillator core, an implementation of the structure of Fig. 2.16

1. It has to destabilize the circuit for oscillation (transfer instability).
2. To guarantee that enough power is fed back to the device input to sustain the oscillation.

As mentioned before, the internal embedding which increases U, generates negative real-part impedance at the input, which avoids absorbing power. Therefore, the second role of the external embedding is quite important. To achieve these two goals, we need to optimize U of the whole structure of Fig. 2.16 all together and not individually, otherwise we might end up with a very active device which is not able to absorb power at its input and thus not capable of sustaining the oscillation.This pair of feedbacks

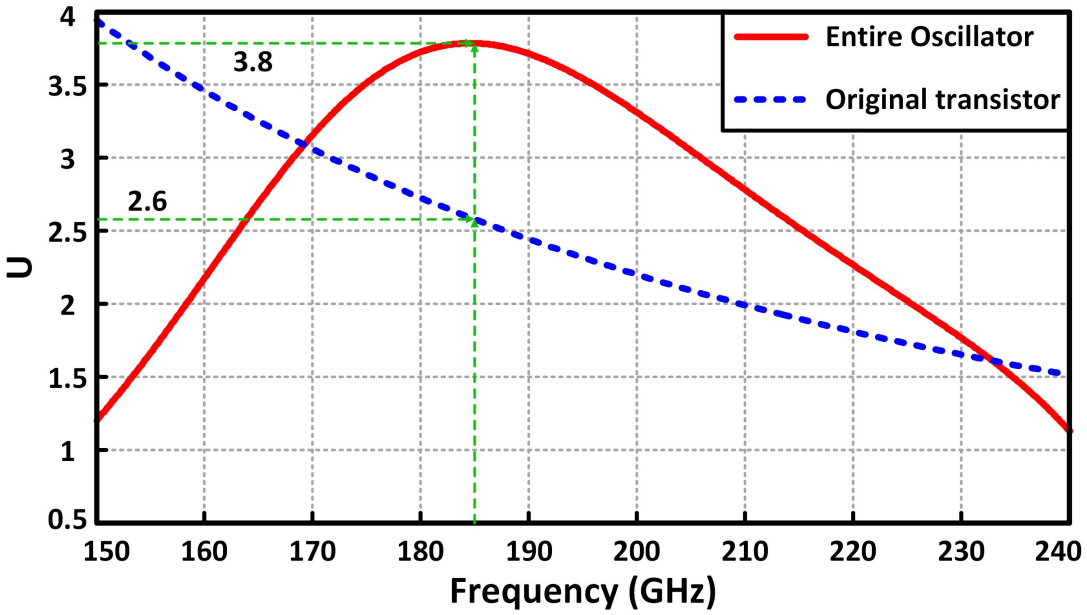

Figure 2.18: Simulated U of the original transistor (2×4.5 μm) and that of the entire oscillator circuit in a 130nm SiGe process. The latter has a peak at the desired frequency.

shapes U to have a peak at the desired frequency as demonstrated in Fig. 2.18 along with the original U of the employed transistor. Beside the fact that by enhancing U the device becomes more active and hence capable of more signal generation, there are two observations that further support our proposed approach of shaping U.

First of all, when the embedding shapes U to peak at the desired frequency, the circuit oscillates very close to that frequency, "as if" there is a resonator that sets the oscillation frequency.

Secondly, there is an intriguing connection between the desired frequency where U is maximized, oscillation frequency, and the maximum efficiency that further justifies our approach. As shown in Fig. 2.19, the frequency of the peak of U is set by the embedding network and not by the transistor size (or bias). Moreover, similar to

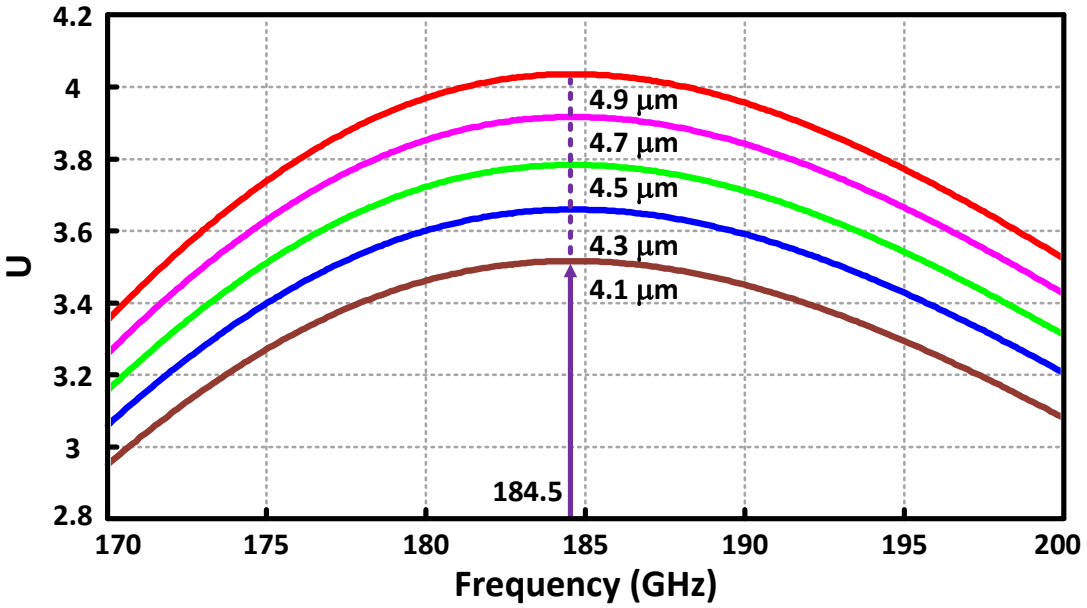

Figure 2.19: Simulated U for the entire oscillator structure for several values of the emitter length and with a fixed embedding in a 130 nm SiGe process

the resonator-based oscillators, the passive structure dominantly sets the oscillation frequency and the transistor only slightly affects it as depicted in Fig. 2.20. As shown in Fig. 2.21, DC-to-RF efficiency of the oscillator becomes maximum if the oscillation frequency is the same as the frequency where U is maximum. Based on these facts, we first design the whole embedding such that U is maximized at the target frequency (see Fig. 2.19). This results in an oscillator with a high efficiency and output power. However, due to the practical implementation issues, the oscillation frequency and the frequency of the peak of U do not coincide. To address this, after designing the complete passive structure, we tweak the transistor size to align these two frequencies. This results in maximum efficiency at the oscillation frequency as shown in Fig. 2.21.

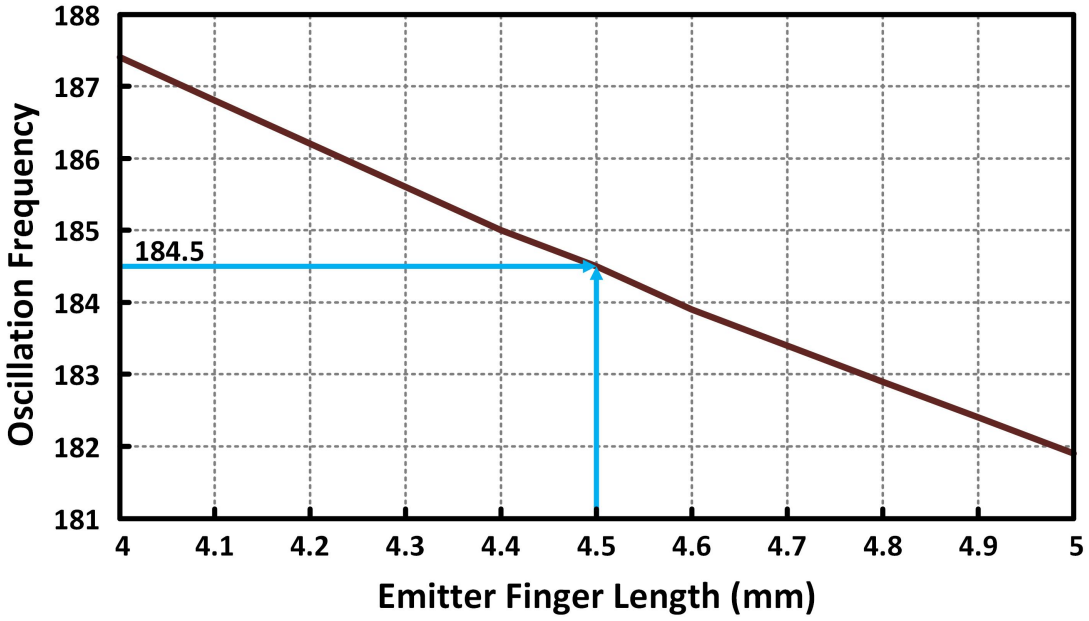

Figure 2.20: Simulated oscillation frequency vs. transistor size (with two fingers) in a 130 nm SiGe process

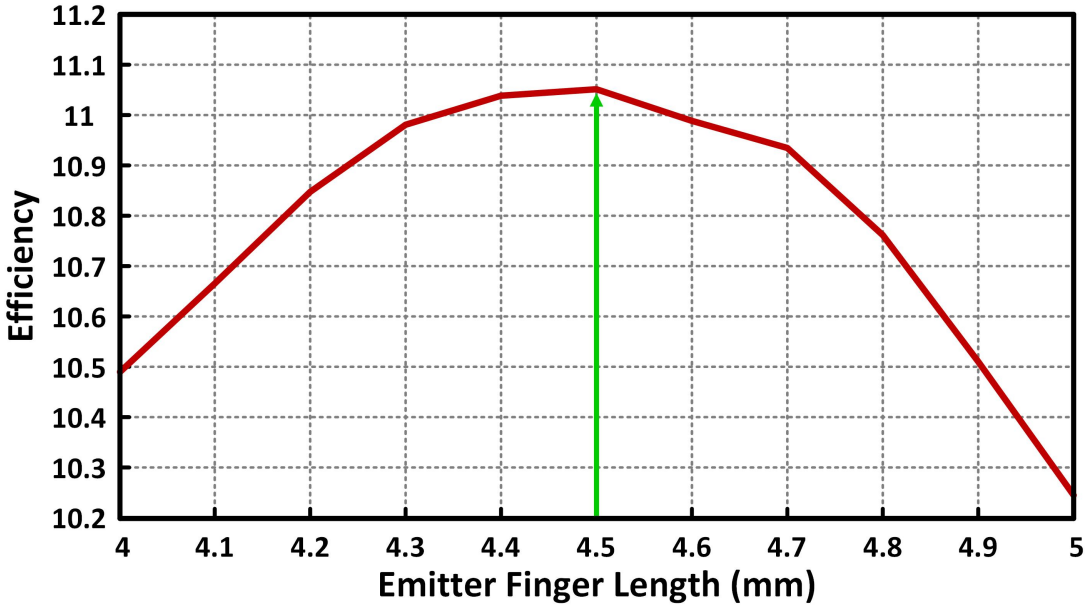

Figure 2.21: Simulated efficiency for different transistor sizes in a 130 nm SiGe process (Total emitter length is twice the value of the horizontal axis)

2.5 Systematic Design and Implementation of an Efficient Fundamental Oscillator Above $f_{max}/2$

In this section we present a method to choose the values of the components of Fig. 2.17 in order to realize the theory introduced in the previous section.

First step is to select the transistor size and bias point.

2.5.1 Step I: Transistor Bias and Size Selection

Since the goal is to shape and maximize U, the device size and bias should be selected such that U of the device is maximized. The unilateral power gain of a transistor is a bias and frequency dependent value. The maximum U of a transistor happens at a certain bias current for different emitter lengths as demonstrated in Fig. 2.22. Usually, as the device size increases, the variation of U versus bias current becomes more flat, i.e. its sensitivity with respect to the bias current decreases (see Fig. 2.22). Meanwhile, the maximum U of the transistor happens at higher bias currents as depicted in Fig. 2.22 and its value decreases as shown in Fig. 2.23. Usually, the bias current is selected either based on the noise performance or the desired output power. In this work the goal is to improve the output power and the power efficiency of the oscillator and hence the bias current is chosen accordingly. Bearing in mind that the maximum power efficiency would be in the order of 10%, the total DC power consumption would be known for a desired output power and hence the bias current and thence, the size of the transistor is selected from Fig. 2.24. Please notice that the DC current of an oscillator might simply increase by 50% when it starts the oscillation and it is loaded. Therefore, the DC power of an oscillator, based on which the transistor is selected and biased can be

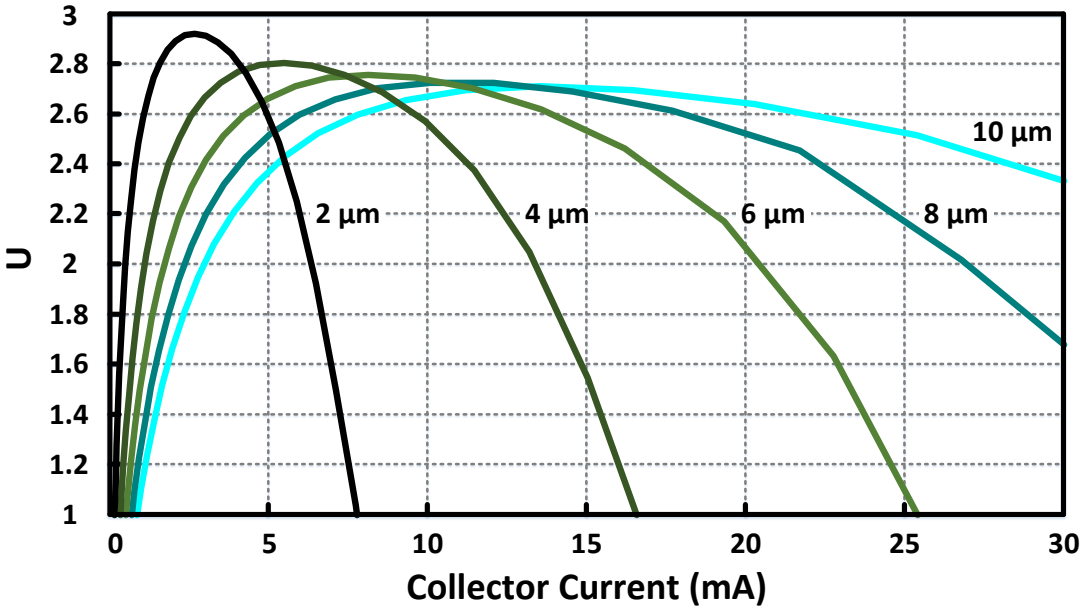

Figure 2.22: U vs. I_c for different total emitter lengths at 180 GHz

quite different than the real values. (This difference can be seen in Cadence simulation by comparing DC current of DC analysis with that of HB or Transient analyses.)

For a selected emitter length, changing the number of emitter fingers, changes the parasitics of the transistor and hence lightly affects U. In this work, based on all the above considerations and trade-offs and to have a maximum output power of around 3 mW, the transistor is chosen to have a total emitter length of 9 μm with two fingers.

2.5.2 Step II: Passive Components Considerations

In the second step, the structure of the passive components are considered. The decoupling capacitor (C_{dcpl}) in Fig. 2.17 is not part of the optimized circuit, because primarily it is used to decouple the DC voltages of collector and base and ideally it should be large

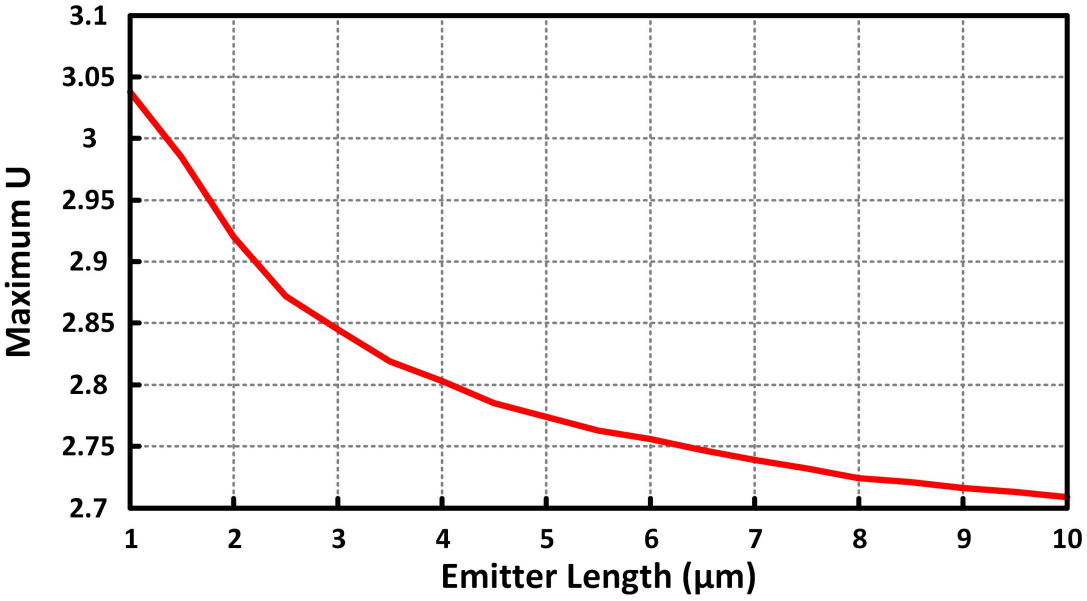

Figure 2.23: Maximum U for different total emitter lengths at 180 GHz

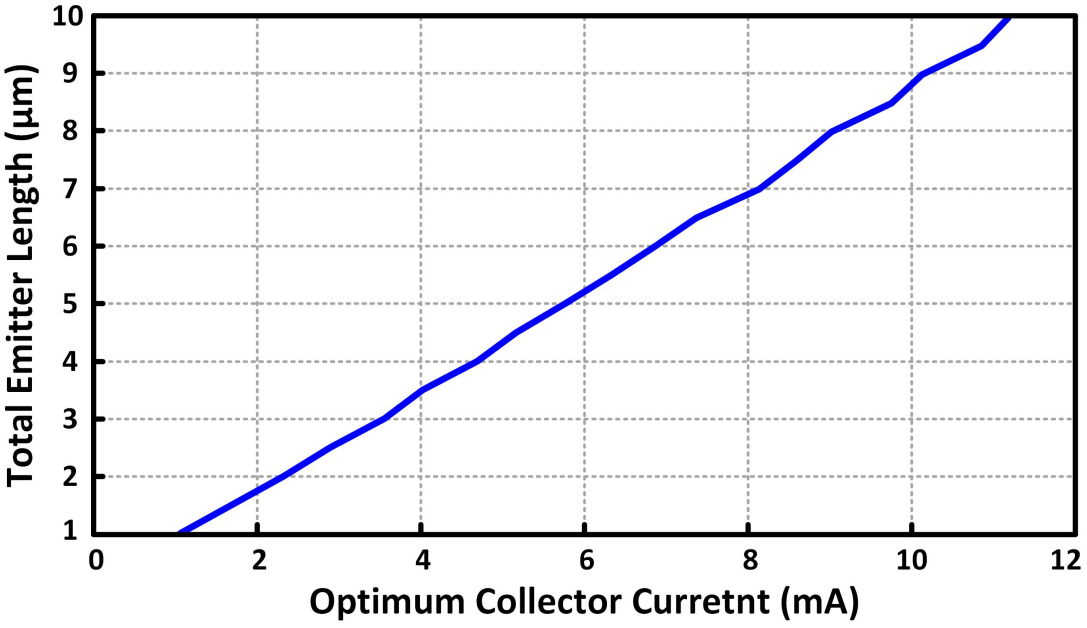

Figure 2.24: Collector current at which U becomes maximum for different total emitter lengths at 180 GHz

enough in order not to affect the impedance of the external feedback. However, to have a reasonable size and avoid poor quality factor which degrades U and the efficiency, it cannot be very large. Moreover, there is another advantage not to have a very large C_{dcpl} that is not short circuit at the desired frequency. In this case, the transmission lines TL_{cb} and TL_b need to be longer to be able to absorb this capacitor. This makes these two transmission lines longer and hence more practical for fabrication at this frequency range. The transmission lines are realized as grounded coplanar wave guides (GCPW) since this structure provides decent shielding at high frequencies [59]. The transmission lines and the decoupling capacitor are carefully simulated in HFSS.

The internal feedback, i.e. the capacitive embedding at emitter along with the choke are also simulated in HFSS. The non-idealities of both components are modeled by the quality factor of the capacitor (C_e) during the design process. According to the EM simulations, the quality factor of the combination of the choke and the capacitor is around 20 at the desired frequency. The choke is realized with a quarter wavelength GCPW transmission line. To decrease energy loss by radiation and also to avoid signal coupling to the substrate and to the rest of the circuit, C_e is realized as a closed box in first and third metal layers and the other plate which lies inside this box is on the second metal layer connected to the emitter. Since the connecting track is very short, the resonance frequency of this capacitor is very high and hence its quality factor is very high even though it is fabricated in lower thin metal layers.

2.5.3 Step III: Optimization

The y-parameters of the selected transistor with the internal feedback (C_e), are extracted from its PDK model. An overall quality factor of 20 (effective quality factor of C_e in

parallel with the choke) is assumed for C_e. The y-parameters of TL_{cb}, TL_b, TL_c and C_{dcpl} are derived from EM simulations in HFSS. All the transmission lines are GCPW's with signal tracks of 3 μm wide, ground walls thickness of 5 μm and the whole width of 50 μm. A set of transmission lines with lengths from 1 μm up to 450 μm (which is beyond half of the wave-length at 185 GHz) are simulated to compose a data table for the optimization solver.

Having the y-parameters of all the components, a code can simply derive the y-parameters of the whole two-port network of Fig. 2.17 and thence the U as a function of the passive components. Given the decoupling capacitor and the data tables of the transmission lines and those of the transistor combined with C_e and the choke, the problem can be formulated as:

$$\textbf{Maximize} \quad U$$

$$\text{by finding} \quad TL_{cb},\ TL_b,\ TL_c \text{ and } C_e$$

$$\textbf{such that:}$$

$$g_{22} \leq 0$$

$$2g_{11}g_{22} - M \leq L,$$

where the input and output ports of the two-port network for which U is maximized are demonstrated in Fig. 2.17 and M and N are defined in Eq. (2.10). The last constraint guarantees the transfer instability to make sure that the circuit is active and generates power while $g_{22} \leq 0$ insures the expected behavior from an output port of the oscillator.

Although the coding of the above optimization problem is straightforward, the problem itself is so nonlinear that *fmincon* in MATLAB has difficulties to solve it efficiently and hence sparse nonlinear optimizer (SNOPT) [60] is used by the code as the solver. The code is supposed to find TL_{cb}, TL_b, TL_c and C_e such that U is maximized at the desired frequency of 185 GHz and the circuit is unstable to sustain the oscillation.

The most subtle part of an optimization-based approach is the ability to consider the sensitivity of the solution with respect to the exploited components while designing. In fact, the circuit might be so sensitive to the values of its components such that a small change in the components might result in a circuit which not only is not optimum but also may not oscillate at all. These changes always happen in reality because of PVT variations and/or modeling errors. Therefore, it must be guaranteed that within a certain error range in the component models, even in the worst case, the network remains unstable and oscillates efficiently. The developed code assumes a reasonable error range for each component. For instance, large capacitors and long transmission lines are assumed to have ±5% error while shorter lines and small capacitors are assumed to bear ±10% error since they are more sensitive to the variations. So the following problem is solved:

$$\max_{TL_{cb},TL_b,TL_c,C_e} \quad \min_i \{U_i\}$$

such that:

$$g_{22_i} \leq 0$$

$$2g_{11_i}\, g_{22_i} - M_i \leq L_i$$

$$i = 1, \ldots, 17.$$

Solving this problem, it is assured that while maximizing the "minimum U" among all corners, all those two-port networks remain unstable to sustain oscillation. Thus, it is guaranteed that even if the worst case happens in reality, the circuit will still oscillate efficiently. This way, the problem of high efficiency oscillator design is formulated as a robust polytopic constrained optimization problem [61] which is implemented as a MATLAB code using efficient practical techniques [62] to be fast and robustly solved.

Remark: It is worthwhile mentioning that none of the above optimization problems

can be solved in a circuit design tool such as Cadence or ADS with sweeping the values of the components. In fact, a nonlinear constrained polytopic optimization problem is a difficult one that has to be solved using sophisticated solvers such as SNOPT.

2.5.4 Step IV: Matching Network

After designing the core oscillator, a matching network should be designed. Since the output voltage and current are closely related to the nonlinearity of the device, the loading is not considered in the previous parts of the design which are based on the small-signal (linear) models. Without considering the non-linearity, it is not possible to know the optimum load for an oscillator. The optimum load of an oscillator can be defined in two ways. Either it is the load that extracts the maximum power from the oscillator, or it is the one that results in the highest DC-to-RF efficiency. In this work since the goal is to improve power efficiency, the optimum load is the latter.

The core oscillator (Fig. 2.17) is designed and optimized for a desired frequency of oscillation, and hence the matching network must not change this frequency. Therefore, it should be designed to be a real load with no imaginary part to avoid changing the frequency. This can be done easily in two steps. First, using Cadence parametric tool, we sweep over different values of a load which is connected directly to the core oscillator (See the left side of Fig. 2.25) and we find the optimum load value for which the DC-to-RF efficiency becomes maximum. Next, using one of the traditional matching networks, such as L-match, the 50 Ω load in parallel to the pad capacitance is brought to the optimal load value that the core oscillator mus be connected to (See the right side of Fig. 2.25). This way, the optimal condition is provided for the core oscillator to attain its best power efficiency.

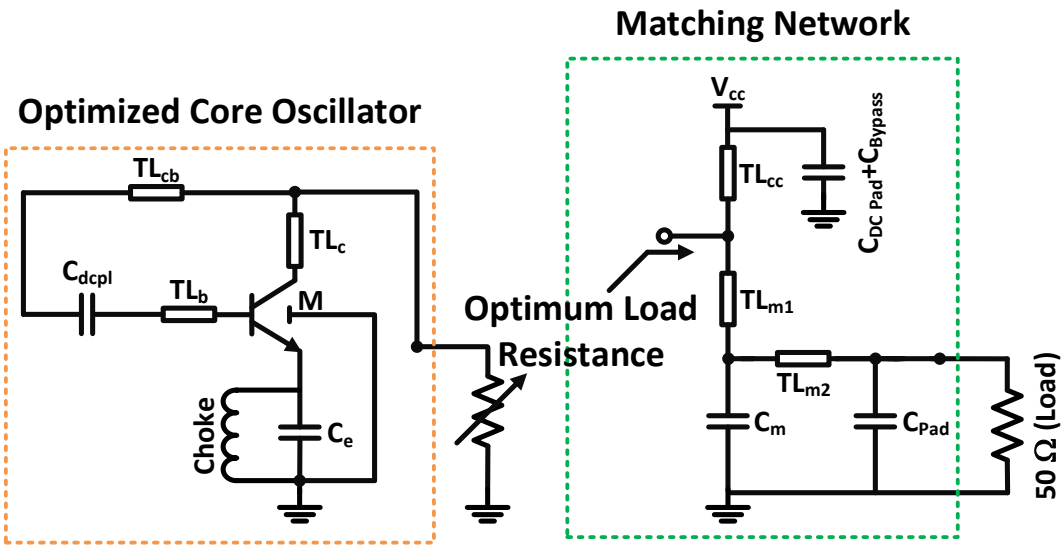

Figure 2.25: Optimum matching network for an oscillator

2.5.5 Design Example

A fundamental oscillator is designed at 185 GHz, employing a 2×4.5 μm HBT in a 130 nm SiGe process as shown in Fig. 2.26. The transistor is biased at the current density where its U is maximum. The problem is solved in MATLAB and results in component values as TL_b= 20.7484 μm, TL_c= 5 μm, TL_{cb}= 30.649 μm and C_e= 15 fF.

The solver has assumed that all transmission lines are straight *GCPW*'s. However none of them are exactly the same GCPWs simulated in HFSS, especially the feedback path composed of TL_{cb}, TL_b and C_{dcpl} is very short and turns back to the transistor and cannot be implemented as straight GCPW with complete walls. Thus, the resulting circuit is not exactly the optimum. Because of all implementation errors, the entire structure has to be re-simulated in HFSS (see Fig. 2.27) to make sure that the resulting y-parameters of the complete structure are close to the one derived by the optimization code. Next, as mentioned in the previous section, by tweaking the transistor size for the

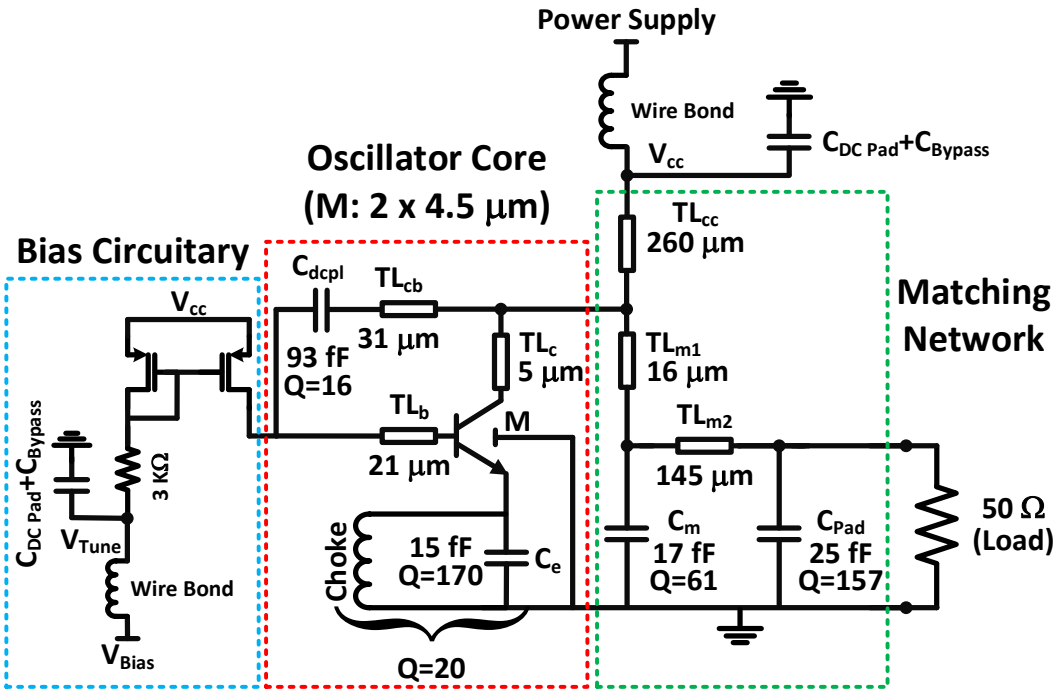

Figure 2.26: Complete oscillator circuit using a 2×4.5 μm HBT transistor

resulting passive structure, we align the oscillation frequency with the frequency of the peak of U to have the best efficiency.

It is useful to mention that the solver has resulted in the lower boundary values for TL_c and C_e, which means that if it was possible to decrease these components, the results might be different and even better. However, a minimum of 5 μm is unavoidable in the layout of TL_c. Besides, we chose not to let the solver go below 15 fF for C_e because of the larger sensitivity in designing small capacitors. Furthermore, the matching network is not considered in the optimization stage and is added to the circuit afterwards.

It is worthwhile mentioning that beside the instability condition based on Eq. 2.9, we have added a set of constraints to assure that all circuits have negative real part of output impedance. This way it is guaranteed that the instability of the resulting circuit

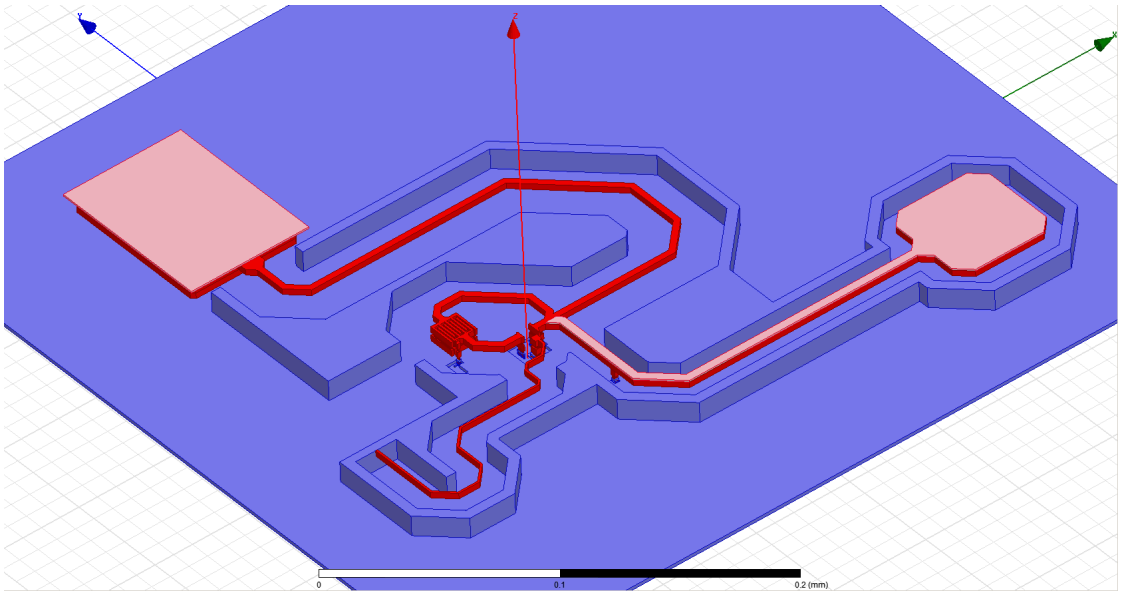

Figure 2.27: The entire structure is EM simulated in HFSS with both supply and signal pads and the shielding ground layer

results in oscillation as expected.

Cadence simulations based on EM simulated models of the whole structure and the post-layout extracted model of the employed transistor show a peak output power of 3.26 mW (with 14.6% power efficiency) and a peak DC-to-RF power efficiency of 15.4% (with 3.1 mW output power) while V_{cc} is 1.8 V. The employed stand-alone transistor has a simulated U of $\simeq$ 2.6 and when the internal/external embeddings are added it increases to $\simeq$ 3.8 (see Fig. 2.18). Note that this increase in U is limited by the loss of passive components. Fig. 2.28 shows the power of fundamental, second and third harmonics at the 50 Ω load and also at the collector node. It is worth mentioning that the output signal at the collector, i.e. before passing through the narrow-band matching network, is a pure sinusoidal. This is a byproduct of the design method which guides all the generated energy into the fundamental frequency rather than the harmonics [63].

Another byproduct of the proposed method is the enhanced phase noise of the re-

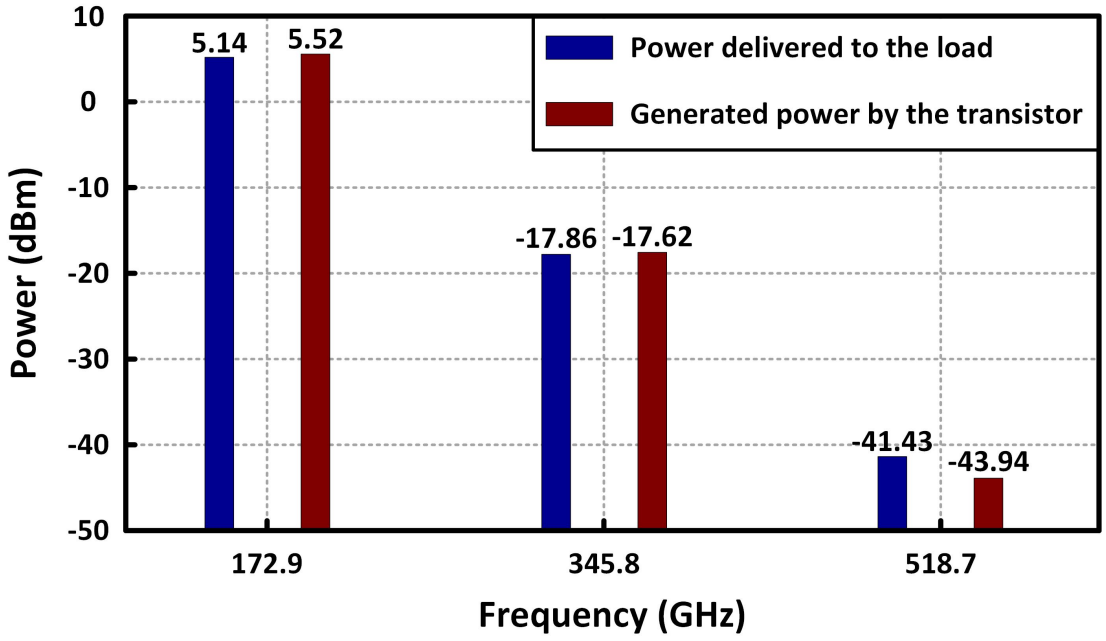

Figure 2.28: Power of the harmonics at the collector node and the 50 Ω load

sulting oscillator. Burning the same DC power, an oscillator with higher DC-to-RF efficiency has a higher output voltage compared to the one with lower efficiency. Thence, the effect of noise on the zero crossings is highly degraded. In other words, for roughly the same amount of noise and DC power consumption, the enhanced SNR improves the phase noise.

2.6 Measurement Results

The designed oscillator is fabricated in a 130nm SiGe:C BiCMOS technology from STMicroelectronics. Fig. 2.29 shows the micro photograph of this oscillator.

The frequency and phase noise measurement setup is shown in Fig. 2.30. The output is probed using a Cascade I220-T-GSG probe. The frequency and phase noise

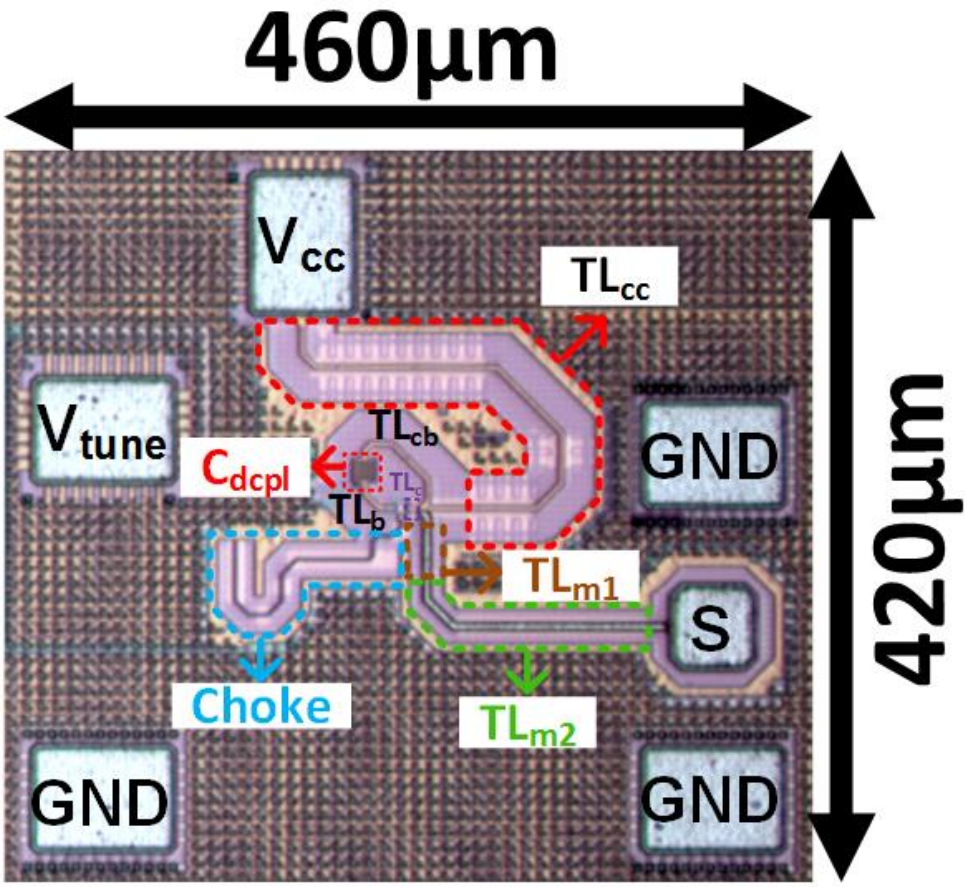

Figure 2.29: Die photo

measurements are performed using a VDI WR5.1 even harmonic mixer (EHM) with 16th harmonic of the LO. The measured oscillation frequency for different V_{tune} and supply voltages are shown in Fig. 2.31. The oscillation frequency can be tuned between 175.3 GHz and 175.9 GHz using the supply voltage and V_{tune} (0.34% tuning range). The best phase noise of -101.7 dBc/Hz and the best figure of merit (FoM) of -195.4 are achieved at 1 MHz offset frequency as shown in Fig. 2.32. The measured phase noise and its FoM versus V_{tune} are depicted in Fig. 2.33 and 2.34. For all measured points,

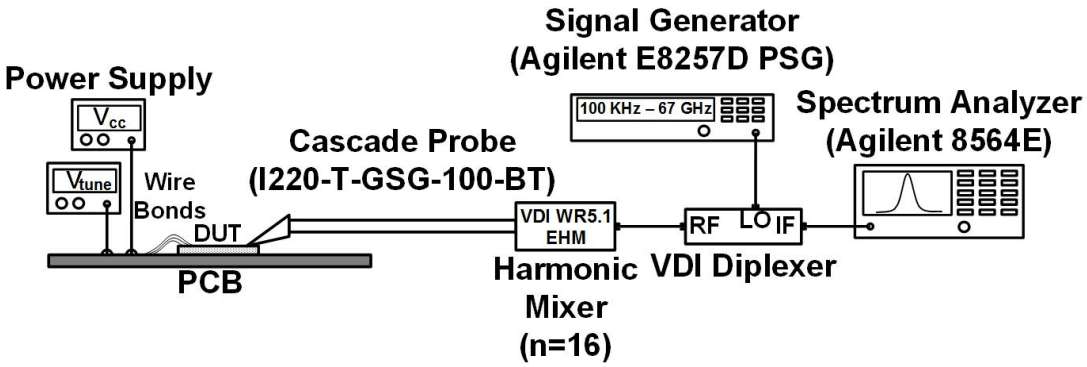

Figure 2.30: Frequency and phase noise measurement setup

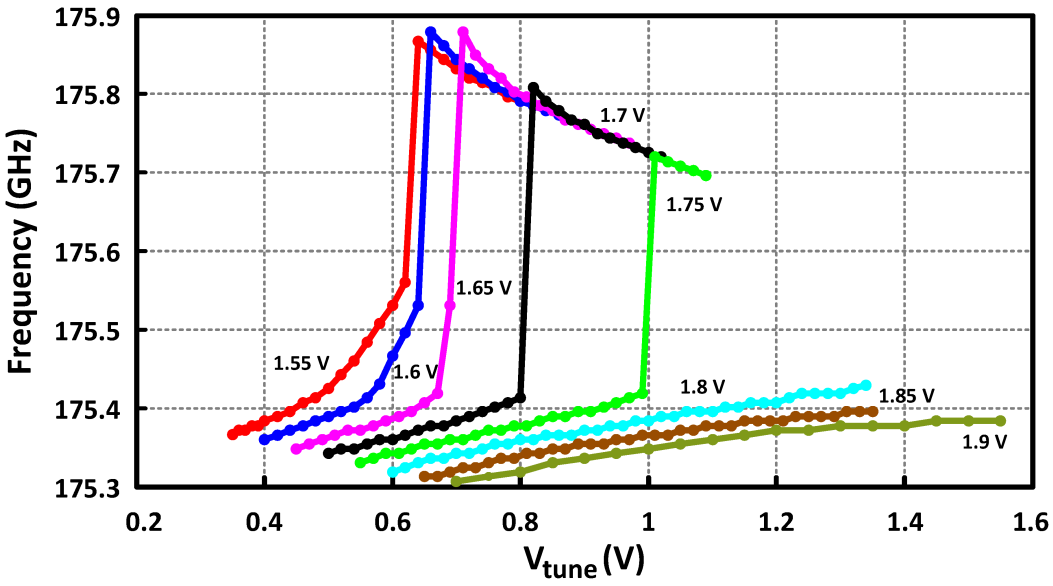

Figure 2.31: Oscillation frequency for different V_{tune} and supply voltages

the phase noise and FoM remain below -90 dBc/Hz and -179 dBc/Hz, respectively. It is worth mentioning that such a decent phase noise is further justified by looking at the poor tuning range of the oscillator with changes in bias and supply voltage (the noise coming through the bias circuitry and the power supply cannot easily cause phase noise otherwise changes in those would result in a much better tuning range).

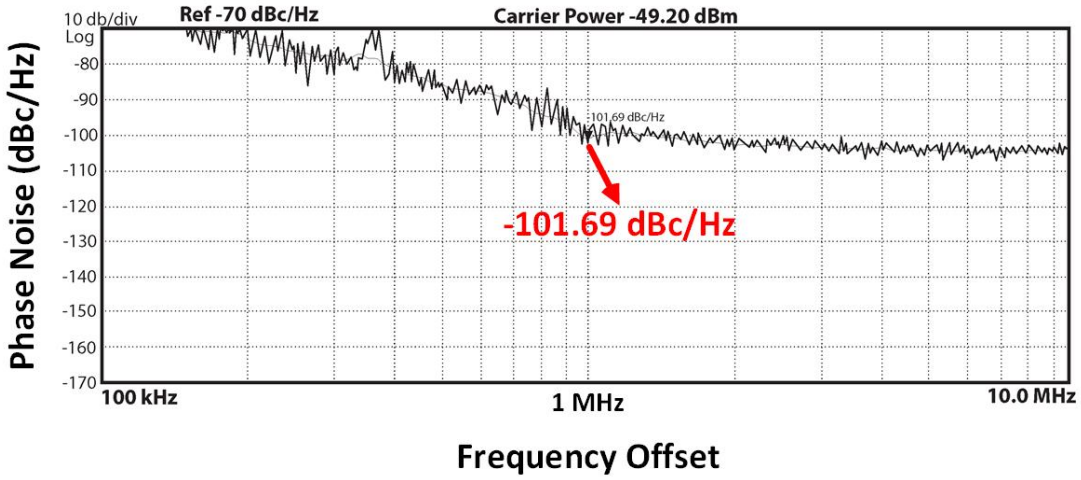

Figure 2.32: Phase noise vs. offset frequency measured using the setup of Fig. 2.30. (The power is not de-embedded.)

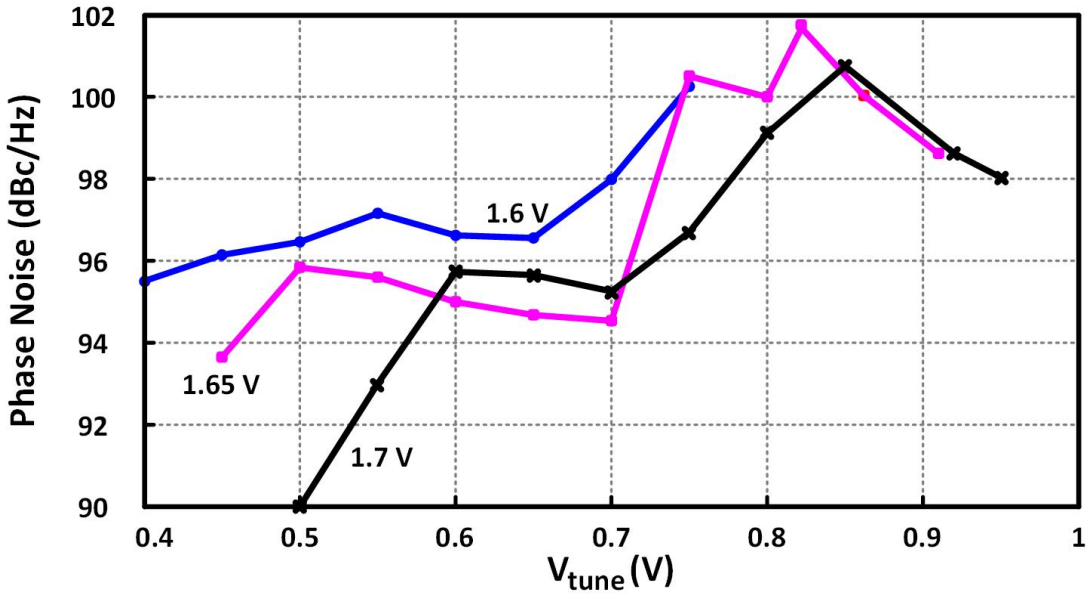

Figure 2.33: Measured phase noise at 1 MHz offset frequency

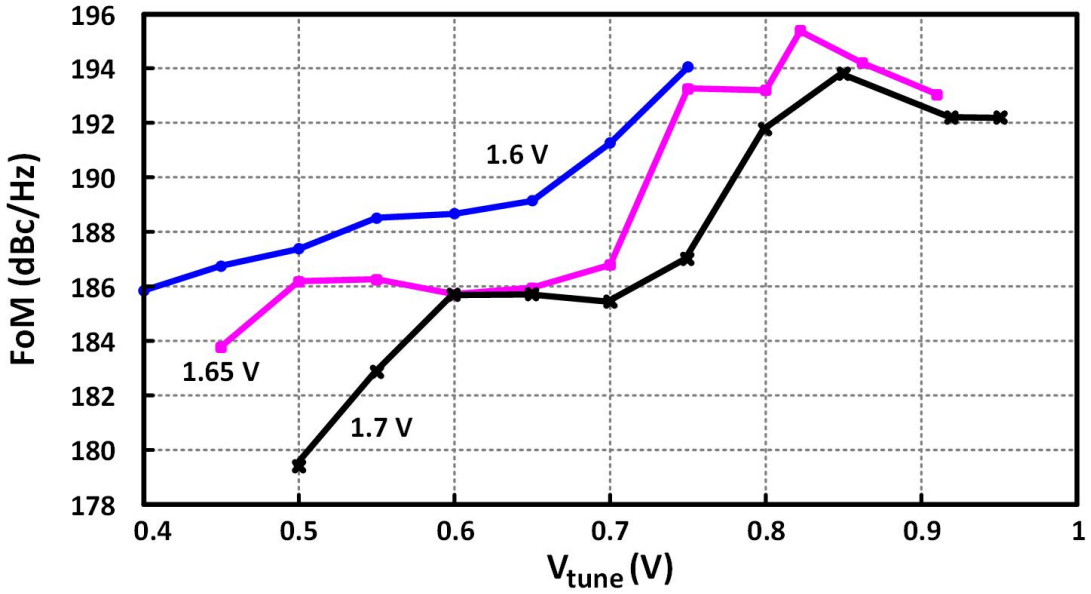

Figure 2.34: Measured phase noise FoM at 1 MHz offset frequency

The Output power is measured using an Erikson PM4 power meter as demonstrated in Fig. 2.35. The loss of the GSG probe and all waveguides is 6 dB, measured carefully by a 500 GHz VNA. Fig. 2.36 illustrates the output power and Fig. 2.37 shows the measured DC-to-RF efficiency for different supply voltages. The maximum output power is 4.8 dBm where the DC-to-RF efficiency is above 9%. The efficiency reaches to a maximum of 11.7%. It is worth mentioning that the oscillator efficiency does not degrade as its output power increases. Namely, for all different supply voltages wherever the output power is the highest, the efficiency is above 8%. For instance, when the power supply is 1.65 V, the maximum output power is 2.57 mW and DC-to-RF efficiency at that point is 10.25%. Table 2.1 compares our results with the state-of-the-art oscillators.

To have a fair comparison in different processes, we also use an efficiency normalized to the value of U at the oscillation frequency. It is defined as

$$\text{Normalized Efficiency} := \frac{\eta}{U} = \eta \times (\frac{f}{f_{max}})^2 = \frac{P_{out}}{P_{DC} \times U}. \tag{2.13}$$

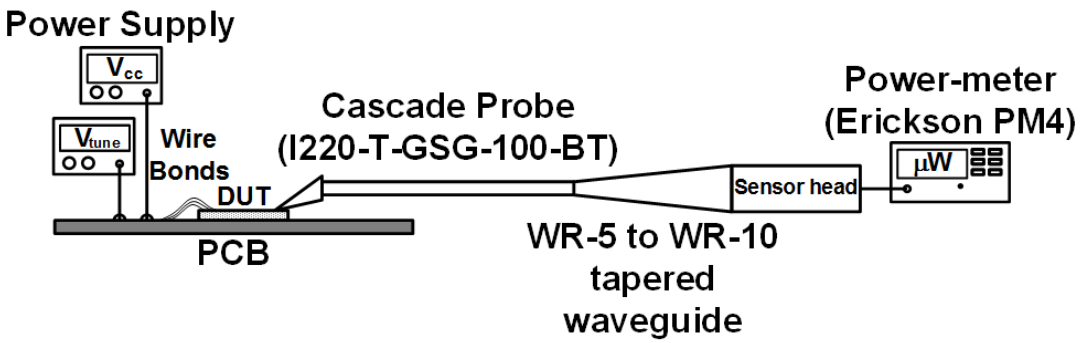

Figure 2.35: Power measurement setup

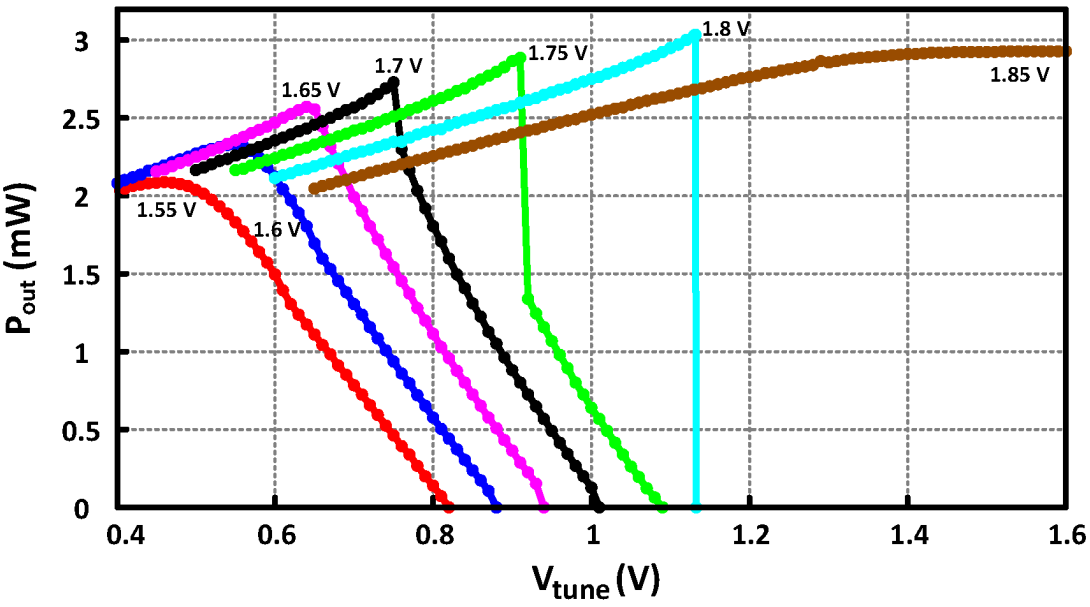

Figure 2.36: Measured output power for several supply voltages (Second chip)

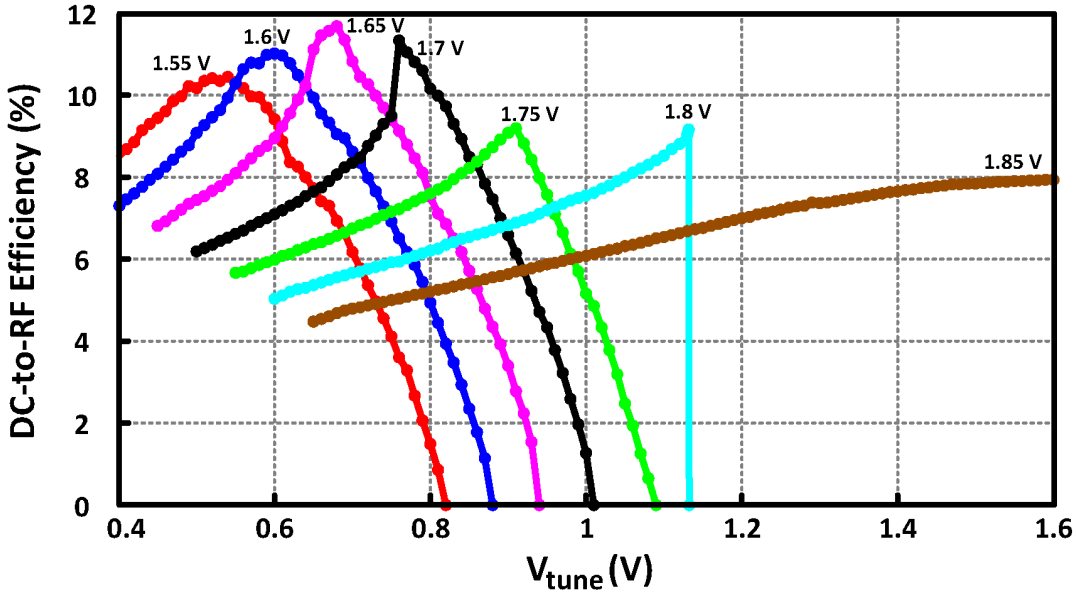

Figure 2.37: Measured DC-to-RF efficiency for several supply voltages (Second chip)

Based on the proposed methods that shows a close relation between the U and the efficiency, given a process with higher U results in a more efficient oscillator. The normalized efficiency takes into account this important fact and compares the oscillators independent of the employed processes.

According to the measurement results, the implemented oscillator not only achieves the highest normalized efficiency, but also the highest output power and DC-to-RF efficiency among all reported oscillators working above $f_{max}/3$ and also the highest FoM at 1 MHz offset among all reported mm-wave oscillators in CMOS/SiGe processes.

An important fact about the designed oscillator is that the frequency, output power and DC-to-RF efficiency between three different measured chips were less than 1% different. This is a direct result of optimizing the worst corner which results in improving all the corners.

Table 2.1: Comparison table

	Technology	Frequency (GHz)	Output Power (dBm)	P_{DC} (mw)	Efficiency ($\eta(\%)$)	f_{max} (GHz)	U @ f_{osc}	Normalized Efficiency ($(\eta/U)(\%)$)	Tuning Range (%)	PN @ 1 MHz (dBc/Hz)	FoM‡ @ 1 MHz (dBc/Hz)
[64]	130 nm SiGe	146.6	-1	47	1.69†	500	11.6	0.145	5.9	-77 @ 5 MHz	150*
[37]	130 nm SiGe	160	-5	231	0.137†	~300	3.5	0.039	2.2	-	-
[29]	160 nm RTD (InP)	164.6	-36.5	0.4	0.056†	-	-	-	1.64	-	-
[32]	250 nm SiGe	165	-15	46.5	0.069†	~435	6.95	0.01	4.7	-79.2 @ 500 KHz	172.7*
[65]	200 nm SiGe	180	-5	120	0.263†	~275	2.33	0.113	2.3	-90	174.3
[38]	130 nm SiGe	184.2	-11	94.9	0.084†	~330	3.21	0.026	2.1	-	-
[66]	45 nm CMOS	189	-27	16.5	0.012†	~300	2.52	0.0048	-	-	-
[33]	90 nm CMOS	196.5	-19	29	0.043†	~160	0.66	0.065	1.4	-	-
[31]	130 nm SiGe	201.5	-7.2	30	0.64	~280	1.93	0.332	3.5	-87	178.3
[31]	130 nm SiGe	212	-7.1	30	0.65	~280	1.74	0.374	2.8	-92	183.7
This	**130 nm SiGe**	**175.6**	**4.8**	**25.8**	**11.7**	**~280**	**2.54**	**4.6**	**0.34**	**-101.7**	**195.4**

‡ Calculated based on $FoM = |PN(f_{offset}) - 20\log(f_{osc}/f_{offset}) + P_{DC}(dBm)|$.

† Efficiency is not provided in the paper and it is not clear if the provided DC power is at the same point where the output power is the maximum or not. So we calculated it by $100 \times \frac{P_{out}}{P_{DC}}$, however in reality their efficiency might be much less than this value.

* Calculated from the given phase noise assuming -20 dB/dec slope.

2.7 Conclusion

A novel systematic approach to design fundamental oscillators above $f_{max}/2$ of the employed transistor is proposed. The idea is to design an embedding, which is composed of two internal and external positive feedbacks such that the unilateral power gain of the network is shaped and maximized at the desired frequency. The resulting oscillator has high output power and efficiency. Using this method, an oscillator close to 2/3 f_{max} of the utilized process is designed which has the highest DC-to-RF efficiency and the best output power and phase noise FoM among all oscillators above $f_{max}/3$.

CHAPTER 3

A 195 GHZ SINGLE-TRANSISTOR FUNDAMENTAL VCO WITH 15.3% DC-TO-RF EFFICIENCY, 4.5 MW OUTPUT POWER, PHASE NOISE FOM OF -197 DBC/HZ AND 1.1% TUNING RANGE IN A 55 NM SIGE PROCESS

A novel approach to design efficient high-output-power fundamental oscillators close to the f_{max} of the employed process is presented. The idea is based on shaping and optimizing the maximally efficient power gain (G_{ME}) of the circuit using a pair of internal/external feedback mechanisms. Solving a constrained optimization problem, an optimum pair of passive feedback network is designed to achieve the highest maximally efficient power gain in order to increase the output power and thence the DC-to-RF efficiency. A 195 GHz fundamental oscillator is designed in a 55 nm SiGe process ($f_{max} \simeq$ 340 GHz), which achieves a significantly higher DC-to-RF efficiency (15.3%) among all reported oscillators working above $f_{max}/3$ of their active devices. The oscillator generates a peak power of 4.5 mW (6.5 dBm) with the best phase noise of -82.3 dBc/Hz and the best FoM of -197 dBc/Hz measured at 100 KHz offset frequency, which is the best phase noise and FoM among all CMOS/SiGe mm-Wave oscillators. The proposed optimization-based method takes into account PVT variations as well as modeling errors of all components in the design process to guarantee the functionality of the fabricated circuit.

3.1 Introduction

High efficiency signal generation is one of the most challenging part of millimeter-wave system design which is needed for many applications such as spectroscopy, imaging and also for high data-rate communication. In fact, power generation in this frequency range is quite difficult since the ability of transistors to generate power degrades drastically

as the frequency approaches the maximum frequency of oscillation (f_{max}). On the other hand, due to the skin effect and being close to the self-resonance frequency of the passive components, power loss is considerably high, which demands sources with high power generation in order to provide reasonable output power for the demanding applications.

Several oscillator structures such as push-push, triple-push and Colpitts have become widespread in RF circuit design whose performances degrade notably as the frequency increases [67]. To design a high DC-to-RF efficiency fundamental oscillator close to the f_{max} of the employed device, new structures and techniques must be adopted. Recently, several millimeter-wave oscillators in SiGe and CMOS processes have been reported [1, 5, 31, 66–68]. The best output power of oscillators working above $f_{max}/3$ of the employed processes is reported to be 2.6 mW by combining the output power of the second harmonic of eight oscillators [5]. The Dc-to-RF efficiency of this oscillator is 1.14%. The highest peak DC-to-RF efficiency is reported to be 2.76% in [67], where the maximum output power is merely 0.5 mW. In this work, a fundamental single-transistor VCO above $f_{max}/2$ of the employed transistor is fabricated in a 55 nm SiGe process that achieves the highest DC-to-RF efficiency of 15.3%, and a maximum output power of 4.5 mW which is the highest among all oscillators working above $f_{max}/3$ of their process, and attains the best phase noise FoM of -197 dBc/Hz measured at 100 KHz frequency offset among all CMOS/BiCMOS mm-wave sources.

In prior arts, to design an efficient oscillator at frequencies close to f_{max}, added output power of the network $P_R = Real\{P_{out} - P_{in}\}$ is targeted for optimization [1,5,40]. However, since the total real power of a two-port network (P_R) cannot be formulated independent of the electrical variables such as the input and/or output voltages of the network [10, 11], instead of P_R, different power-related functions of the network are maximized [1,5,11], none of which guarantees the optimality of P_R.

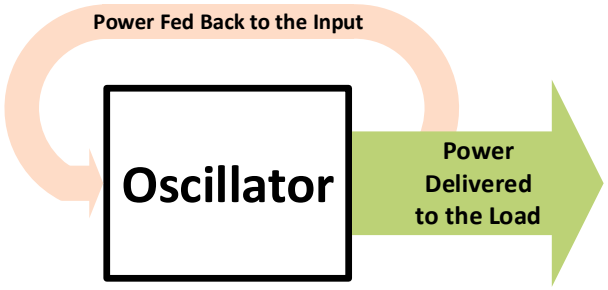

Figure 3.1: Power amplification point of view for an oscillator

In this work, a new approach for designing high efficiency and high output power oscillators close to the f_{max} of the employed process is proposed. The systematic optimization-based method is introduced in Section 3.2. The implementation along with the measurement results are described in Section 3.3. And finally, Section 3.4 summarizes this work.

3.2 High Efficiency Oscillator Design

An oscillator can be seen as a network that amplifies the power, feeds part of it back to its own input to be amplified and delivers the excess power to the load (Fig. 3.1).

From this point of view, an efficient high output power oscillator is composed of a decent amplifier which amplifies part of its own output power and delivers the rest to the load. Therefore, to design a high efficiency oscillator, its power gain must be maximized. Meanwhile, the resulting network must be unstable and thence, traditional power gains which are defined for stable networks cannot be employed. However, beside the unilateral power gain which is a measure for the activity of a two-port network (and is shaped and optimized in [6] to increase the efficiency of oscillators beyond the $f_{max}/2$

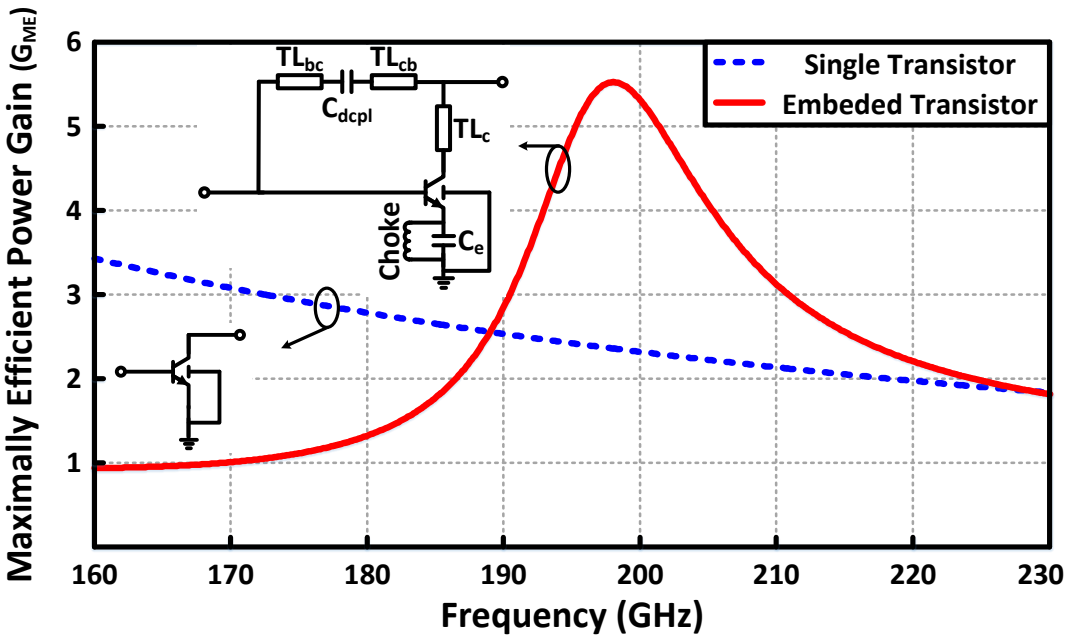

Figure 3.2: Shaped and maximized G_{ME} at the desired frequency

of the employed transistor), there exists a power gain which is well-defined for two-port networks and remains meaningful even if the network is unstable. Maximally efficient power gain, G_{ME}, is an old figure of merit for active two-port networks which is basically defined in order to have a power gain which remains finite and well-behaved both for stable and unstable networks [48]. It is claimed that an amplifier designed based on

$$G_{ME} = \frac{|y_{21}|^2 - |y_{12}|^2}{4g_{11}g_{22} - 2Re(y_{12}y_{21}) - 2|y_{12}|^2}, \tag{3.1}$$

has a better large signal performance and dynamic range compared to the one designed based on maximum available gain G_{MA} [48]. The maximally efficient power gain is defined in order to have an optimized added-power gain which makes it a reasonable measure to be optimized for an oscillator. These features are in particular very important for oscillators since they are unstable networks that work in large signal regime.

In this work, the maximally efficient power gain of the network is shaped and maxi-

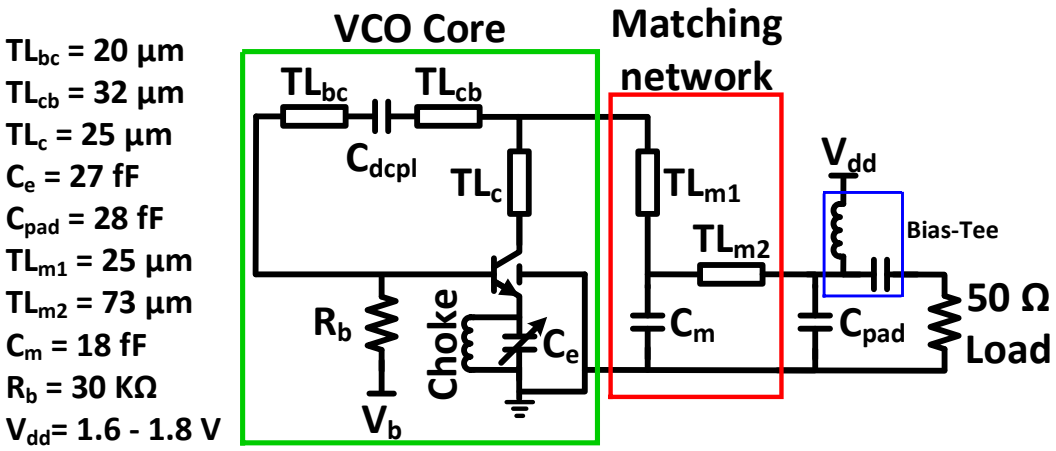

Figure 3.3: Complete VCO with the matching network. C_e is a varactor controlled by V_{ctrl}.

mized (see Fig. 3.2) at the desired oscillation frequency while the circuit is kept unstable to ensure oscillation. In order to optimize G_{ME}, a feedback loop composed of three pieces of transmission lines (TL_{bc}, TL_{cb} and TL_c) and a decoupling capacitor (C_{dcpl}) between them, in addition to C_e, a degeneration capacitor (similar to a Colpitts oscillator) are employed. The capacitive degeneration also forms a positive feedback which results in a circuit with less loss (by compensating part of the network loss by introducing negative resistance at base) which is desired for a high efficiency oscillator. At the final stage, this capacitor is replaced by a differential varactor in order to be able to change the oscillation frequency. The positive inductive feedback destabilizes the circuit and feeds back part of the output power to the input for sustainable oscillation. This feedback is composed of three TL's and a decoupling capacitor between them in order to provide enough degree of freedom at both input and output ports (Fig. 3.3). It is worth mentioning that since the TL's are not lumped components, it is not possible to swap TL_{cb} and TL_{bc} as it can be done for lumped series components. The role of TL_c is vital to introduce an appropriate phase shift to the signal at the collector. Moreover,

a decoupling capacitor with a reasonable capacitance made in this process has a resonance frequency close to the desired oscillation frequency which makes the design very sensitive to its model. In order to desensitize the performance of the circuit with respect to the variation of C_{dcpl}, by utilizing multiple long fingers and connecting two top metal layers, the resonance frequency of this capacitor is intentionally decreased much below the oscillation frequency such that it becomes an inductor (with a reasonable quality factor) at the oscillation frequency. The TL's dimensions must be designed such that they introduce minimum loss to the circuit. The width of the conducting track of all TL's is chosen to be 1.5 μm which corresponds to the minimum α/Z_0 [59] at the oscillation frequency, based on EM simulations (α is the real part of the propagation constant and Z_0 is the characteristic impedance of the TL).

Similar to having a resonator, an active unstable two-port network oscillates close to the frequency where its G_{ME} is maximized. This emphasizes on the power amplification point of view for an oscillator and justifies the suggested approach to shape and optimize G_{ME}. The values of the utilized components are found using an optimization code in MATLAB which exploits SNOPT as a solver. The code guarantees that all considered corners of the circuit remain unstable and the worst G_{ME} among all corners is maximized. Using the y-parameters of each component and their corners, the design is formulated as a non-convex constrained optimization problem. To make sure that the resulting circuit will behave as an oscillator, it is important to make sure that it is unstable at the output port, i.e. the real part of its output impedance is negative. This is easily done by including the proper constraints to the optimization problem. Since the problem is a non-convex constrained optimization, the solution might be very sensitive such that a very small deviation from the optimum solution may result in a circuit that might be very inefficient or not oscillate at all (this is one of the many reasons that it is not possible to do such a design using Cadence parametric tool). In order to overcome

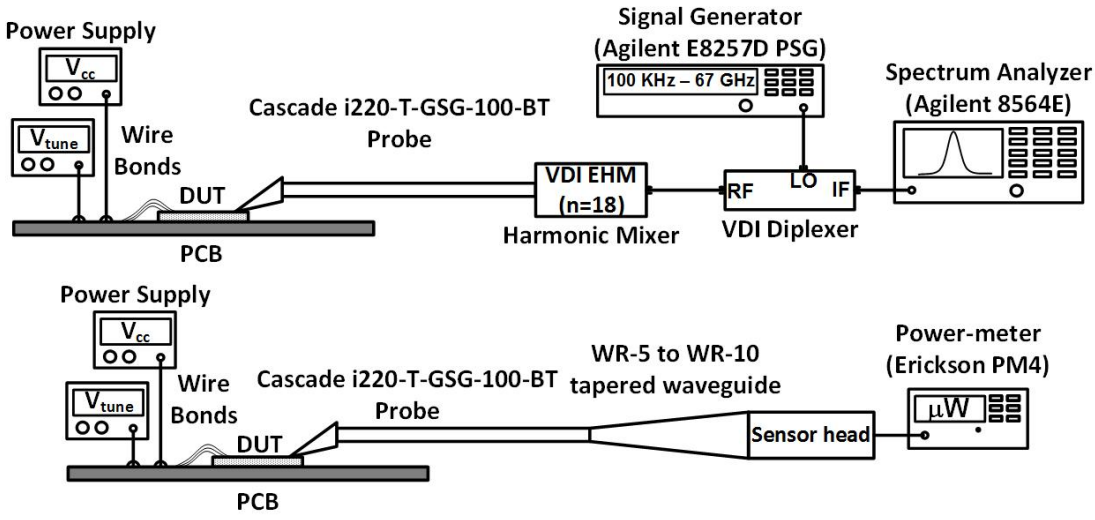

Figure 3.4: Top: Frequency and Phase noise measurement setup, Bottom: Power measurement setup

this basic issue, a reasonable modeling error and precision range for each component are considered in addition to the fast and slow corners of the transistor. Next, the code is written such that the solver maximizes the minimum G_{ME} among all corners while satisfying the instability and behavioral constraints.

3.3 Measurement Results

The frequency and power measurement setups are shown in Fig. 3.4. In order to measure the frequency and the phase noise the output is down-converted using an even harmonic mixer (EHM) with 18th harmonic of the LO. The phase noise results and FoM measured at 100 KHz and 1 MHz offset frequencies are shown in Fig. 3.6 for different values of V_{ctrl} and a two plots of phase noise measurement are shown in Fig. 3.5. The best phase noise/FoM of -82.3/-197 dBc/Hz are achieved at 100 KHz offset and -98.6/-193.3 dBc/Hz at 1 MHz offset. The phase noise FoM remains below -188 dBc/Hz for

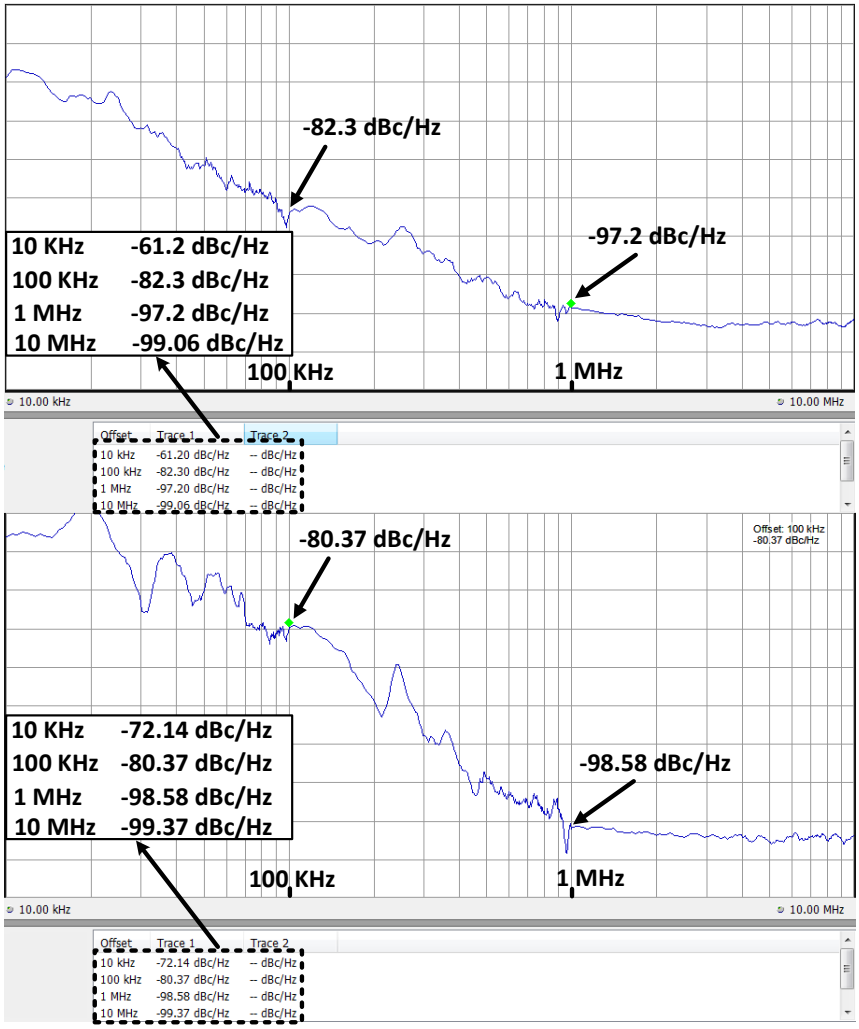

Figure 3.5: Two samples of phase noise measurement

all measured points for both offsets. The oscillation frequency can be tuned by V_{ctrl} between 194.2 GHz and 196.4 GHz (1.1% tuning range) as shown in Fig. 3.7 where the die photo is also demonstrated.

The Output power is measured using Erikson PM4 power meter as shown in Fig. 3.4. Fig. 3.8 depicts the measured output power and DC-to-RF efficiency for different supply voltages and collector currents. The maximum output power is 6.5 dBm and the efficiency reaches to a maximum of 15.3 %. It is worth mentioning that the DC-to-RF

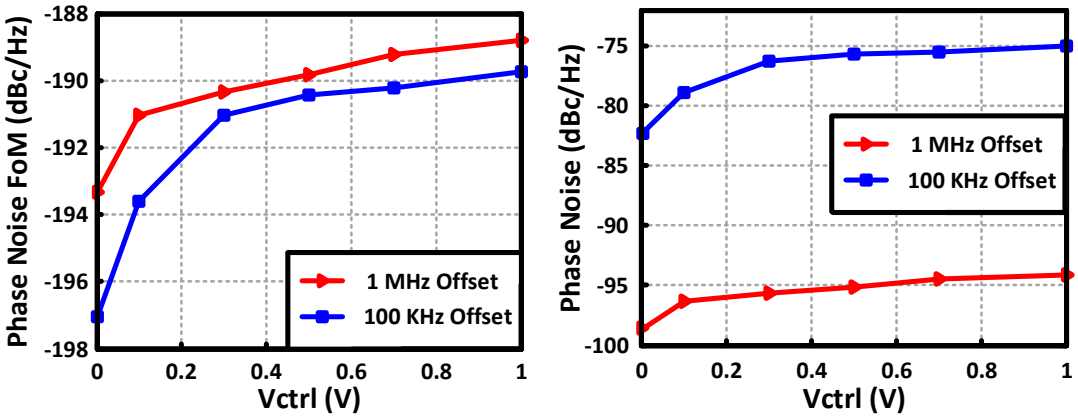

Figure 3.6: Measured phase noise and FoM vs. V_{ctrl}

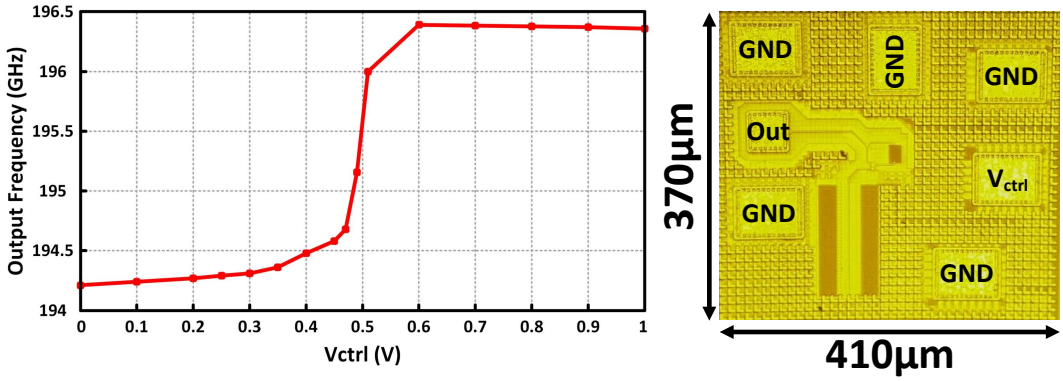

Figure 3.7: Measured tuning range and the die photo

efficiency improves as the output power increases, which is not a common characteristic of the signal generators. Table 3.1 compares this work with the previous state of the art oscillators. According to the measurement results, this VCO achieves the highest output power and DC-to-RF efficiency among all reported oscillators working above $f_{max}/3$ and also the highest FoM at both 1 MHz and 100 KHz frequency offset among all reported CMOS/BiCMOS mm-wave oscillators.

Table 3.1: Comparison table

	Technology	Freq. (GHz)	**Output Power** (dBm)	**Efficiency** (%)	Tuning Range (%)	**PN @ 100 KHz** (dBc/Hz)	**|FoM|† @ 100 KHz** (dBc/Hz)	**PN @ 1 MHz** (dBc/Hz)	**|FoM|† @ 1 MHz** (dBc/Hz)	**Power-Area Efficiency** (mW/mm^2)
[65]	200 nm SiGe	180	-5	0.263	0.55	-	-	-90	174.3*	2
[38]	130 nm SiGe	184.2	-11	0.084	2.1	-	-	-	-	-
[66]	45 nm CMOS	189	-27	0.012	-	-	-	-	-	0.02
[68]	130 nm SiGe	190.5	-2.1	0.34	20.7	-	-	-82.64*	165.6*	2.5
[31]	130 nm SiGe	201.5	-7.2	0.64	3.5	-	-	-87	178.3	2.6
[38]	130 nm SiGe	209	-25	0.0063	-	-	-	-	-	-
[69]	130 nm SiGe	210	1.4	2.4	10.6	-63	173*	-87.5	179	51.1
[5]	65 nm CMOS	256	4.1	1.14	4.3	-	-	-94	178.6	7.7
This	55 nm SiGe	**195**	**6.5**	**15.3**	**1.1**	**-82.3**	**197**	**-98.6**	**193.3**	**84.4**

‡ Calculated based on $FoM = PN(f_{offset}) - 20\log(f_{osc}/f_{offset}) + P_{DC}(dBm)$.

* Roughly calculated from the provided data.

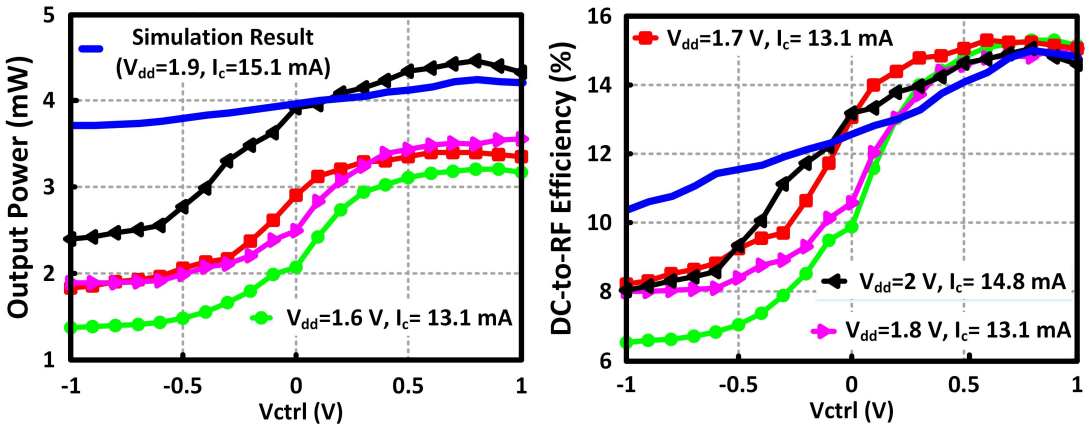

Figure 3.8: Simulated and Measured output power and DC-to-RF efficiency

3.4 Conclusion

In this work, a novel systematic method of designing high efficiency VCO's beyond the $f_{max}/3$ is proposed. The efficacy of the proposed method is proved by designing a 195 GHz VCO whose output power, DC-to-RF efficiency, phase noise and its FoM are the highest among all VCO's above the $f_{max}/3$ of the employed transistors.

CHAPTER 4

A 173 GHZ AMPLIFIER WITH 18.5 DB POWER GAIN IN A 130 NM SIGE PROCESS: SYSTEMATIC DESIGN OF HIGH-GAIN AMPLIFIERS ABOVE $F_{MAX}/2$

A novel theory of stability for two-port networks is developed. Using this theory, a new method of designing amplifiers with high power gain working close to the maximum frequency of oscillation (f_{max}) is proposed. Contrary to the existing amplifier design methodologies, in this method the transistor capability of power amplification is fully utilized. This becomes more important at frequencies close to the f_{max} where having high power gain is challenging due to degraded activity of the employed device. The proposed method considers the modeling errors and process-voltage-temperature (PVT) variations of the employed components in the design stage to ensure that the fabricated amplifier will be stable with a decent power gain even if the worst case variations and modeling errors happen. To show the feasibility of the proposed approach, a three-stage amplifier at 173 GHz, using BJT's from a 130 nm SiGe process is designed. The fabricated amplifier has a maximum measured power gain of 18.5 dB at 173 GHz. A similar three stage amplifier using the same transistors with the same bias, would give a maximum gain of 6.8 dB in simulation, assuming perfect lossless conjugate matching at input, output and between stages. So it is clear that the fabricated amplifier achieves a significant improvement over the power gain.

4.1 Introduction

Millimeter-wave (mm-wave) and Terahertz (THz) systems promise many attractive applications in different areas [14, 16, 20–22, 25, 70]. However, there are many challenges toward the implementation of these systems. In particular, the passive components are

more lossy in these frequency ranges due to the skin effect and also operating close to their self-resonance frequency. Thus, it is vital to design amplifiers with decent power gain in these frequency ranges. More importantly, as frequency approaches the f_{max}, the activity of the device decreases and hence its ability for power generation and amplification degrades [6, 10]. Therefore, high power generation and/or high power gain at high frequencies is a hard goal to achieve. The degradation of activity can be observed by studying the unilateral power gain of the device (U), which is the activity Figure of Merit (FoM) [8]. U decreases by a slope of 20 dB/dec above the $f_{max}/2$ [38], and reaches 0 dB at f_{max}, beyond which the device is no longer capable of power amplification/generation. In addition to its invariance which makes it an inherent value of a two-port network, the importance of U stems from the fact that the maximum transducer power gain (G_C) of a stable two-port network (which is the most practical and useful measure of power gain [57]), is limited by $(\sqrt{U} + \sqrt{U-1})^2$ [10].

There is a trade-off between the power gain and stability. Since solid-state circuits are strongly affected by many types of variations, being too close to the stability boundary without considering the potential errors and variations is quite risky and it is possible that the fabricated circuit has a poor power gain or becomes unstable and hence either oscillates or saturates independent of the input signal [10]. In addition, the real part of the input impedance and/or output impedance diminishes by getting closer to the stability boundary, which results in a more lousy and lossy matching network. A lossy matching network can provide conjugate matching merely from one side and hence degrades the transducer power gain both by its loss and by its incomplete matching.

In recent years, researchers have tried to come up with new methods to overcome the challenges in mm-wave and THz power amplification. As a first step, there has been an ongoing research in the device fabrication technologies in order to increase f_{max}

[71]. Others have tried to carefully design the amplifiers and their matching networks to achieve higher power gain from each employed device [37, 72, 73].

To the best of our knowledge, the only systematic approach to design a mm-wave amplifier is the so-called unilateralization [54, 74–79]. The main idea in this method is to eliminate the reverse signal path from the output to the input. In this case, the maximum transducer power gain becomes equal to the unilateral power gain of the circuit ($G_C = U$). A unilateralized device not only usually has a better power gain than the original device, but also becomes stable and SCM would be possible. An internal unilateralization technique is introduced in [76] and verified by implementing a 50 GHz amplifier with 20 dB power gain. A transformer based feedback for unilateralization is proposed in [77] and an amplifier working at 46 GHz with 18.3 dB power gain is fabricated. A unilateralization method is employed in [79] to design an amplifier with 22.5 dB power gain at 233 GHz. However, none of these works achieved a power gain of more than $0.51 \times U$ which can be explained by the loss of passives and matching networks and more importantly it is due to variations and modeling errors. Although unilateralization is used in amplifier design, it suffers from four major issues. The first and the foremost important one is that this method results in wasting the capability of the transistor which is able to produce higher power gain ($(\sqrt{U} + \sqrt{U-1})^2$) than what targeted ($U$). The second issue is that the elimination of the reverse path to the input is usually narrow band and hence the bandwidth of the resulting amplifier is very limited. Third, none of the proposed methods of unilateralization are capable of considering the corners and variations of the components which results in much lower gain than expected ($0.51 \times U$ at best which is achieved by [79]). Finally, at the design stage, all the suggested methods assume that the passives are lossless which is an unreasonable assumption at high frequencies.

There is a heuristic approach whose results are closer to unilateralized power gain compared to the works where unilateralization has been targeted [10,80]. This approach maximizes a power related function in order to achieve a high power gain. In fact, instead of the power gain, the real part of $(P_{out} - P_{in})/(|V_{in}V_{out}|)$ is maximized, which means there is no guarantee that this method can always result in a reasonable power gain. Besides, it is never possible to guarantee the optimality conditions in this method. In particular, it demands for a constant phase shift and voltage gain across the device, none of which can be easily satisfied in an amplifier. Besides, the optimality conditions demand for a constant phase shift and voltage gain across the device, none of which can be easily satisfied in an amplifier. The amplifier is designed using sweeping tool in Cadence and does not satisfy any of the optimality conditions.

In this paper, a novel stability region is derived based on which a new method for designing high power gain amplifier at frequencies above $f_{max}/2$ is proposed. This method takes into account the variations, modeling errors and losses of the components in the design stage and maximizes the power gain while the stability is guaranteed. The rest of this paper is organized as follows. Some basics of two-port networks are reviewed in Section 4.2. A novel stability theory for two-port networks is established in Section 4.3, based on which, in Section 4.4 a design methodology is proposed and a high power gain amplifier is designed in a 130 nm SiGe process. The measurement results are shown in Section 4.5 which prove the efficacy of the proposed method. Finally, Section 4.6 concludes this work.

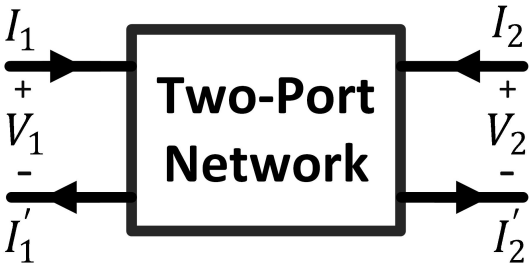

Figure 4.1: Two-port network

4.2 Basics of Two-Port Networks

In this section, some basic properties of two-port networks are reviewed based on which the proposed method of designing a high power gain amplifier will be explained. A two-port network, can be represented by its admittance parameters:

$$\begin{aligned} I_1 &= y_{11}V_1 + y_{12}V_2 \\ I_2 &= y_{21}V_1 + y_{22}V_2, \end{aligned} \tag{4.1}$$

while $I_1 = I_1'$ and $I_2 = I_2'$ (see Fig. 4.1) [56]. Two important properties of these networks, i.e. *Activity* and *Stability* can be stated using these parameters.

4.2.1 Activity and Stability

A two-port network is active at a desired frequency if the total real power flowing into the network is negative at that frequency. In other words, it is active if it is capable of power amplification or oscillation [10]. Using the y-parameters, the complex power flowing into the network can be expressed as (see Fig. 4.1):

$$P = P_R + jP_I = V_1I_1^* + V_2I_2^* = y_{11}^*|V_1|^2 + y_{22}^*|V_2|^2 + y_{12}^*V_1V_2^* + y_{21}^*V_1^*V_2. \tag{4.2}$$

In order to be active, P_R has to be negative.

Activity is a necessary condition for instability [56]. A two-port network is unconditionally stable at a desired frequency if it remains stable for all passive terminations connected to its input and output ports [57]. It can be shown that a two-port network is stable for all possible passive terminations if these three conditions are simultaneously satisfied [10]:

$$g_{11} \geq 0, \tag{4.3}$$

$$g_{22} \geq 0, 1 \tag{4.4}$$

$$2g_{11}g_{22} - M \geq L, \tag{4.5}$$

where $M + jN = y_{12}y_{21}$, $L = |y_{12}y_{21}|$ and $y_{ik} = g_{ik} + jb_{ik}$. The first two inequalities are satisfied for most active devices especially at frequencies close to f_{max} and hence, potential instability of a transistor is usually caused by the failure to satisfy the third one.

4.2.2 Power Gains

The performance of an amplifier cannot be fully described without considering its peripherals. Namely, both internal characteristics such as activity and stability, and also the connected source and load are important in this regard. Several different power gains are defined in the literature. Here, three important power gains of a two-port network are reviewed.

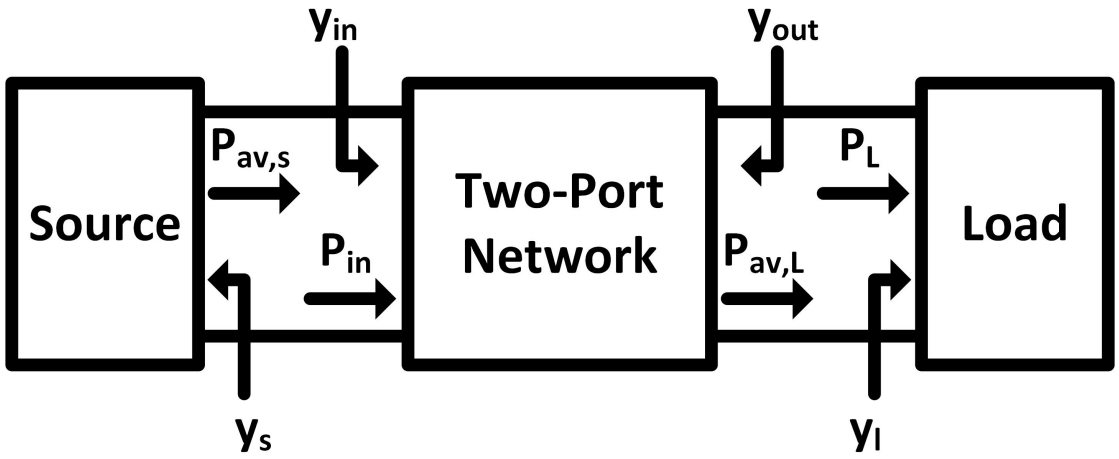

Figure 4.2: Transducer Power Gain Definition

4.2.2.1 Transducer Power Gain (G_T) and Maximum Stable Power Gain (G_{msg})

The most meaningful measure of a two-port network as an amplifier is its transducer power gain (since it takes into account matching at both input and output ports) [57]:

$$G_T := \frac{P_L}{P_{av,s}} = \frac{4|y_{21}|^2 g_s g_l}{|(y_{11} + y_s)(y_{22} + y_l) - y_{12}y_{21}|^2}, \tag{4.6}$$

where $g_s = \mathrm{Re}(y_s)$, $g_l = \mathrm{Re}(y_l)$, $P_{av,s}$ is the available source power and P_L is the power delivered to the load (see Fig. 4.2).

At high frequencies where obtaining a high output power and gain is quite challenging, an amplifier must achieve the largest possible G_T which necessitates simultaneous conjugate matching (SCM), i.e. conjugate matching at both input and output ports (i.e. $y_s = y_{in}^*$ and $y_l = y_{out}^*$). SCM is necessary for an amplifier in order to receive the maximum power from the source ($P_{in} = P_{av,s}$) and also to deliver the maximum power to the load ($P_L = P_{av,L}$) (see Fig. 4.2).

The following source and load admittances provide SCM [10] :

$$g_s = R \times g_{11}, \quad b_s = -b_{11} + \frac{N}{2g_{22}}, \tag{4.7}$$

$$g_l = R \times g_{22}, \quad b_l = -b_{22} + \frac{N}{2g_{11}}, \tag{4.8}$$

where

$$R = \sqrt{1 - \frac{M}{g_{11}g_{22}} - \frac{N^2}{4g_{11}^2 g_{22}^2}}.$$

Remark: SCM is possible only if the network is unconditionally stable and in that case R is real [10, 81, 82].

In case of SCM, G_T is denoted by G_C and can be derived from (4.6) as:

$$G_C = \frac{|y_{21}|^2}{2g_{11}g_{22}(1+R) - M} = \frac{|A|}{\eta + \sqrt{\eta^2 - 1}} \tag{4.9}$$

where

$$A = \frac{y_{21}}{y_{12}} = \frac{s_{21}}{s_{12}}, \tag{4.10}$$

is a complex number whose absolute value is the so-called "maximum stable power gain" (G_{msg}), and

$$\eta = (2g_{11}g_{22} - M)/L,$$

is the well-known Rollet's stability factor ($\eta > 1$ means unconditional stability and $\eta < 1$ translates to potential instability [83]).

Equation (4.9) indicates that G_C, which is defined only where the network is unconditionally stable, is always less than $G_{msg} = |A|$ and at the edge of instability (i.e. where $\eta = 1$), G_C simply becomes equal to $|A|$, which explains the term *maximum stable gain* (see Fig. 4.3). Besides, as depicted in Fig. 4.3, G_C becomes unity at $f = f_{max}$ which is exactly where U also becomes unity. However, at this frequency $|A|$ is equal to

$$\eta + \sqrt{\eta^2 - 1},$$

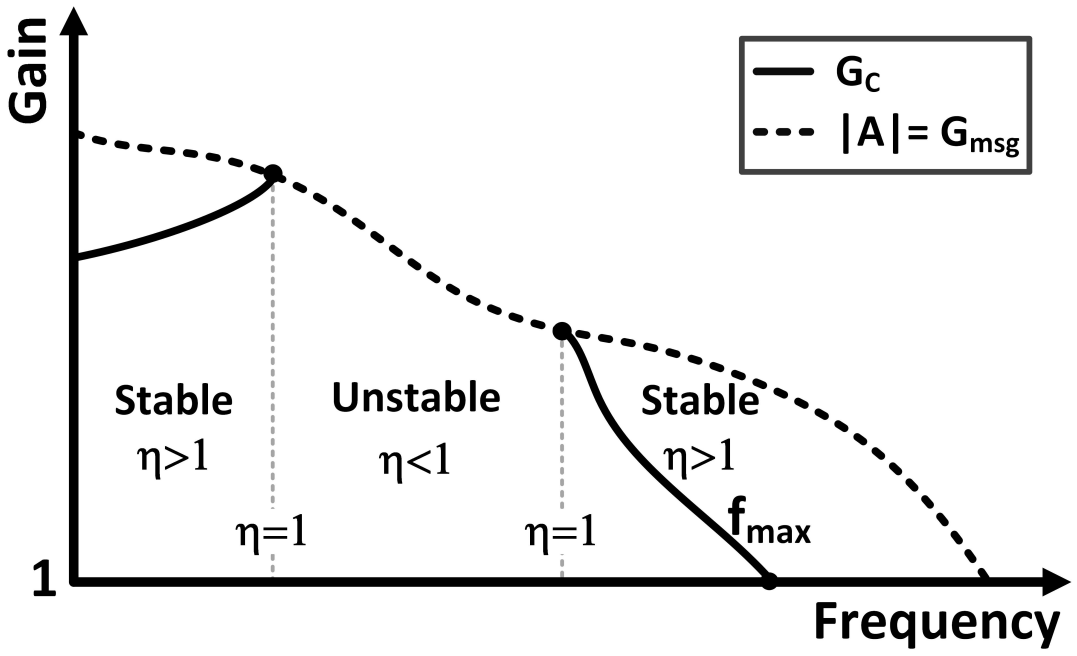

Figure 4.3: G_C and G_{msg} and stability intervals versus frequency

which might be much larger than unity. This is why $|A|$ is not a measure of activity or power gain of a two-port network (in contrary to G_T and U). Nevertheless, A is an inherent characteristic of the network, which is invariant with respect to being cascaded with linear-lossless-reciprocal two-port networks.

4.2.2.2 Unilateral Power Gain

The unilateral power gain a.k.a. ***Mason's invariant*** represents the transfer activity ($4g_{11}g_{22} < |y_{21} + y_{12}^*|^2$) of a two-port network and can be expressed using y-parameters [8]:

$$U := \frac{|y_{21} - y_{12}|^2}{4(g_{11}g_{22} - g_{12}g_{21})}, \tag{4.11}$$

which is a real number that depends on bias and frequency and is the activity FoM. The two-port network is active if $U > 1$ (and if $U < 0$).

Activity of the device and hence its U decreases monotonically at high frequencies. For the transistors in CMOS and SiGe processes, U is approximately 6 dB at $f_{max}/2$ and decreases by a slope of 20 dB/dec (6 dB/oct) and becomes unity at f_{max}. Therefore, since the power amplification and signal generation are closely related to the activity of the device, in this last active frequency octave, signal generation and power amplification is a major challenge.

The activity FoM, has useful properties such as:

I. It is invariant under any four-port linear-lossless-reciprocal (FPLLR) embedding [8].

II. The transducer power gain of a unilateral ($y_{12} = 0$ or equivalently $s_{12} = 0$) two-port network, which is simultaneously conjugate-matched at both ports, is equal to its U [8, 54]. This is why U is called the "*unilateral power gain*".

III. The maximum theoretical transducer power gain that an SCM two-port network can provide depends only on U [10]:

$$G_{Cmax} = (\sqrt{U} + \sqrt{U-1})^2 \tag{4.12}$$

It is always possible to render a non-unilateral two-port network *unilateral* at a desired frequency by an appropriate FPLLR embedding [54]. As mentioned before, such an embedding preserves the value of U but not necessarily A and G_C. This important feature enables us to increase G_C using FPLLR embeddings. It is also possible to employ a lossy embedding to change G_C. However, a lossy embedding usually decreases the activity of the network and hence degrades U and thence G_{Cmax}.

In the next section, the relation between G_C, A and U is carefully studied which results in a novel convex stability region for the two-port networks.

4.3 Gain Plane, Stability Region and Normalized Gain Loci

As mentioned in the previous section, G_C, U and A are three related power gains of a two-port network. Although G_C is the maximum of G_T (if SCM), it can be improved (using FPLLR embedding) since unlike U, it is not a network invariant. Combining (4.9) and (4.11) results in [10]:

$$\sqrt{\frac{G_C}{U}} = \left|\frac{A - G_C}{A - 1}\right|. \tag{4.13}$$

This is a fundamental equation relating the three power gains of a two-port network. The advantage of (4.13) over (4.9) is that U and A can be controlled independently. Namely, A can be modified by FPLLR embeddings (which contain feedback) while U is preserved, and if necessary, U can be simply modified while A is kept constant, by adding loss to the input and/or output ports [10, 58]. On the contrary, there is no clear way to modify η and A separately and thence (4.9) cannot be utilized for this purpose.

In the following, (4.13) is studied thoroughly to obtain an intuition and a graphical tool to study power gain and stability of two-port networks.

4.3.1 Gain Plane

A two-dimensional mapping of (4.13) provides us with a very useful graphical tool to study the stability and the power gain of a two-port network. Bearing in mind that A can

be varied while U is preserved, (4.13) can be written as:

$$\sqrt{\frac{G_C}{U}} = \left| \frac{1 - \frac{G_C}{U}\frac{U}{A}}{1 - \frac{1}{U}\frac{U}{A}} \right|. \tag{4.14}$$

where the ***normalized gain***, i.e. $k = G_C/U$ is expressed as a function of the complex number U/A. Therefore, a plane (*the gain plane*) with coordinate axes $x = Re(U/A)$ and $y = Im(U/A)$ is exploited to locate the unique loci of constant normalized gain. Moreover, since G_C is defined only when the network is unconditionally stable, it is necessary to determine the stability region in this plane. This stability region along with the constant G_C loci provides a powerful graphical tool to observe the performance of a two-port network as an amplifier. Furthermore, the convex region of stability and the constant gain loci which are derived in the following, are employed in this work within a nonlinear optimization code to design a stable amplifier which provides the maximum possible power gain for all design corners.

4.3.2 Stability Region

A new convex stability region in the gain plane is introduced in this part. In contrary to the well-known $k - \Delta$ stability test [57], this new region shows how close/far the network is to become unstable. As mentioned before, at the boundary of stability $\eta = 1$ and hence $G_C = |A|$. Substituting this into (4.14), defines the boundary of the stability region in the gain plane as follows:

$$x^2 + y^2 = 2(U - U^2)x - U^2 + 2U^4(1 - \sqrt{\frac{U^3 - 2Ux + 2x - U}{U^3}}). \tag{4.15}$$

This stability boundary is shown in Fig. 4.4 along with the locus of $|A| = 1$ which is a circle. It is clear that outside this circle the network is not of any interest since the forward gain is less than the backward gain.

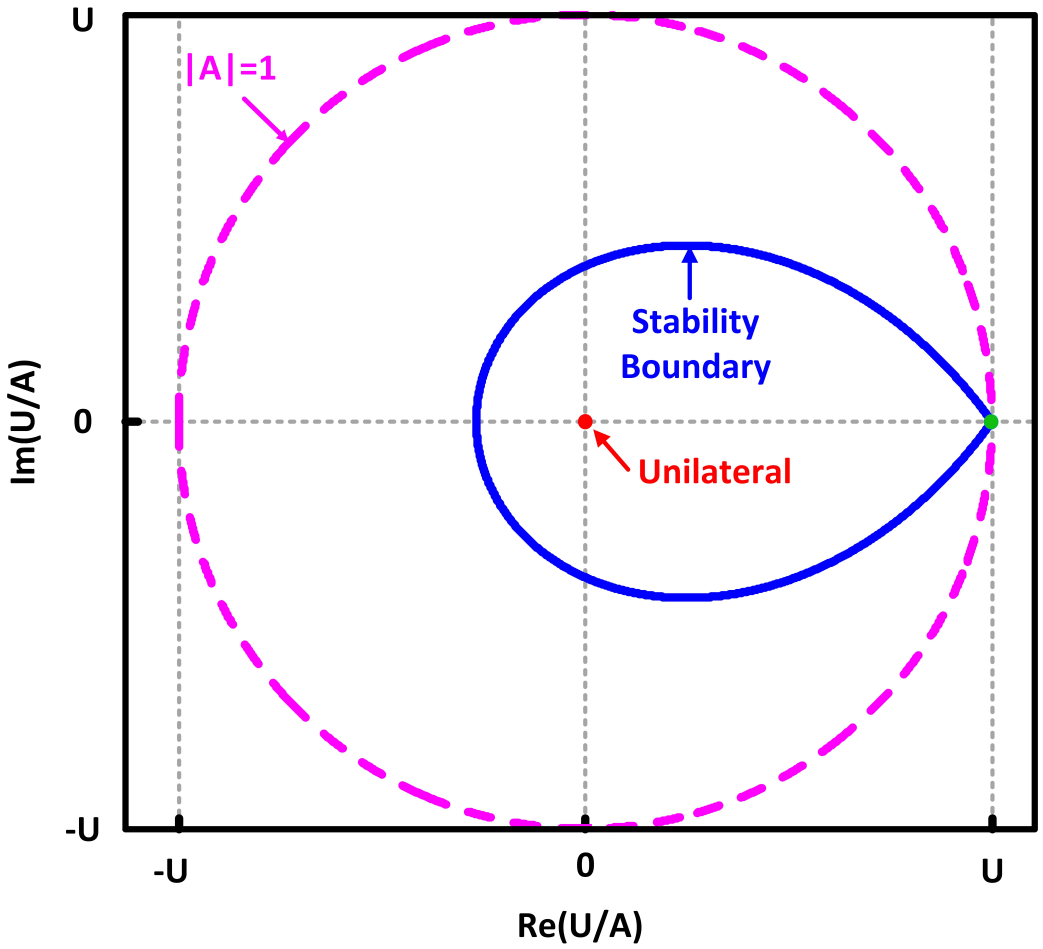

Figure 4.4: The stability region in the gain plane is *inside* the blue boundary (solid). Outside the pink circle (dashed) the device is not useful anymore since $|A| < 1$.

4.3.3 Normalized Gain Loci

Similar to the previous derivation, by substituting $G_C = kU$ in (4.14), it is possible to show that for a fixed *normalized gain* "k", the loci in the gain plane are part of the following circles that lies inside the stability region :

$$(k^2 - \frac{k}{U^2})y^2 + (1 - kx)^2 = k(1 - \frac{x}{U})^2. \tag{4.16}$$

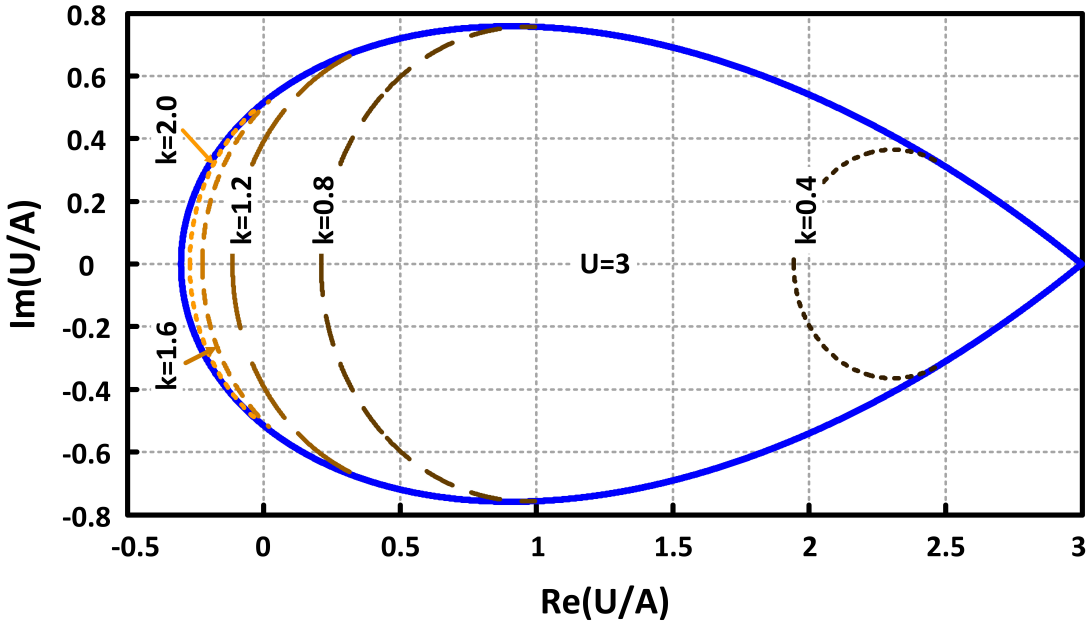

Figure 4.5: Constant normalized gain (k) loci in the *gain plane* depicted for $U = 3$

Fig. 4.5 depicts a few of these constant gain circles. The normalized gain is greater than k_0 on the left side of the k_0 constant circle.

A complete set of derived equations of stability boundary, constant gain loci and their intercept points are given in Appendix.

Having the y-parameters of a two-port network at a desired frequency, we are able to calculate its unilateral power gain (U) from (4.11), its maximum stable gain (A) from (4.10) and thence, the real and imaginary parts of U/A. Therefore, we can map the network into the gain plane and see if it is stable or not and how far from the boundary it is. When it is stable, the given network lies on a constant normalized gain circle of (4.16) where $G_C = k \times U$.

It is worth emphasizing that the existence of the constant normalized gain loci (or similarly the constant G_C loci since $k = G_C/U$ and U is constant under FPLLR embed-

dings), once more depicts the fact that a two-port network with higher U can provide higher G_C.

Remark 1: The origin of the gain plane corresponds to the *unilateral* network where $G_C = U$ as depicted in Fig. 4.4 (see Appendix). Also, examining the loci of $G_C = 1 \times U$ reveals that there are infinite number of points in the gain plane that result in the same power gain as unilateralization which do not require to satisfy unilateralization condition ($y_{12} = 0$), i.e. there is no need to cancel the feedback from the output to the input.

Remark 2: $G_{Cmax} = (\sqrt{U} + \sqrt{(U-1)})^2$ corresponds to the far left intercept point on the boundary of the stability region and the x-axis (see Appendix). This is the maximum possible transducer power gain of a two-port network having unilateral power gain of U, under SCM condition. In case $U \gg 1$, $G_{Cmax} \simeq 4 \times U$, which is a well-known limit of G_C at low frequencies.

Remark 3: Careful examination of Fig. 4.5, constant gain circles and their interceptions with the stability boundary reveals that in contrary to common belief, being close to instability does not necessarily result in a high gain. *To have a high gain we need to be on the left side of the stability region.*

This new plane proves more efficient for amplifier design compared to Smith Chart, since it provides loci for constant transducer power gain if SCM, whereas in Smith Chart there is no such concept for G_T.

Remark 4: *It is worth mentioning that there are constant gain circles for the available power gain (G_{av}) and also for the operational power gain (G_P) in Smith Chart [57, 82] that should not be mixed up with the constant G_C loci in this approach. Those constant gain circles in Smith Chart show the gain variation based on the choice of the load or source impedances and reaching to the center of those circles is equivalent*

to obtaining a gain equal to the G_C of the given transistor. However, in this proposed method, using an FPLLR embedding the G_C of the transistor is improved by moving towards left side (to the high gain regions) of the stability region in the gain plane. Next, since stability is assured by remaining inside the introduced region of Fig. 4.4, using SCM, the amplifier would come up with a gain equal to this improved G_C.

Remark 5: Although the presented stability region is derived from the equations containing Rollet's factor (K_f), there are two main advantages in this rigorous graphical presentation. First, a convex stability region is introduced which significantly helps, compared to the set defined by $K_f > 1$, to build a well-behaved constraint for a constrained optimization problem which makes it possible to be solved by the existing optimization solvers. In fact, convexifying a problem is a well-known trend in control system theory to make an optimization problem solvable using advanced optimization techniques [84]. The proposed theory provides a convex constraint for the stability of two-port network, whereas the set defined by $K_f > 1$ is a non-convex nonlinear constraint which is strongly misbehaved constraint. Second, the graphical tool in this work makes this theory quite useful for designers to get intuition about the network stability and its sensitivity to changes in different parameters, whereas having $K_f = 10$ or $K_f = 2$, does not provide any insight about how close or far from stability boundary the circuit is and it even does not imply that the former is more stable than the latter. Whereas in the proposed stability plane, the designer can see the movements of the network in the plane caused by the embeddings, parasitics and corners to have a solid understanding about sensitivity of the network with respect to those parameters.

Fig. 4.6 shows how a transistor with emitter length of $2 \times 5\mu$m (and properly biased) in the employed process evolves in the gain plane as the frequency changes from 55 GHz to 180 GHz. As the frequency increases towards f_{max}, the device becomes stable

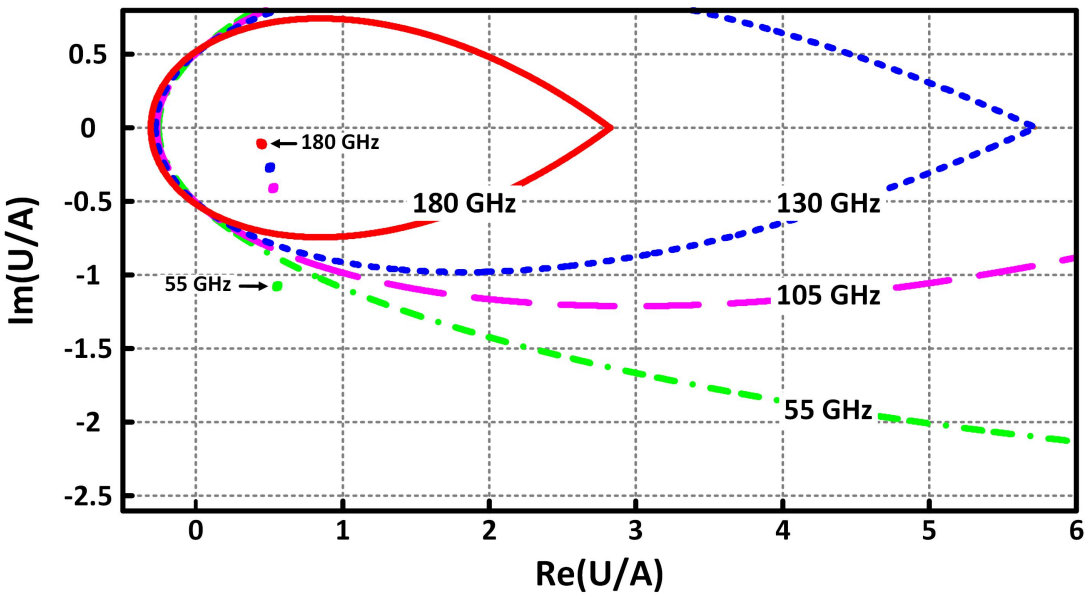

Figure 4.6: As frequency increases from 55 GHz to 180 GHz, stability region shrinks and the transistor moves inside stability region.

and U decreases which results in a smaller stability region as depicted in Fig. 4.6.

4.4 High Power Gain Amplifier Design

In this part, a new method to design a high power gain amplifier is suggested. By providing enough degrees of freedom for an FPLLR embedding similar to Fig. 4.7, it is possible to move a two-port active network over the gain plane towards the left to improve k while U is constant.

In order to design a high power gain amplifier, first of all, the transistors and their bias points should be selected.

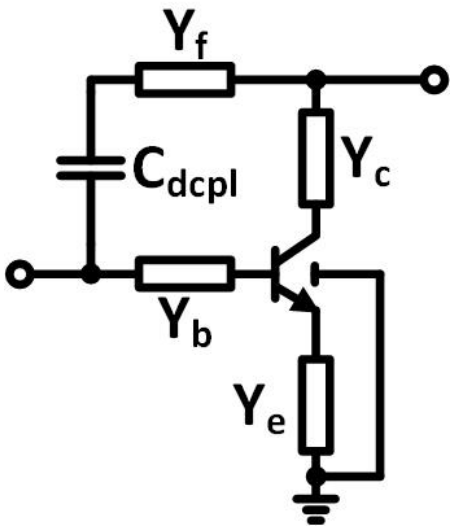

Figure 4.7: Proposed FPLLR embedding which provides enough degree of freedom to move the circuit towards high gain region.

4.4.1 Step I: Transistor and Bias Selection

Since the power gain of an amplifier is closely related to its unilateral power gain, the device size and bias should be selected such that its U is maximized. Usually, as the device size (the emitter length of a bipolar transistor in this case) increases, its maximum U decreases (see Fig. 4.8). Meanwhile, as the size increases, the maximum U of the transistor happens at higher bias currents (see Fig. 4.9) and becomes more flat, i.e. its sensitivity with respect to the bias current decreases (see Fig. 4.10).

The noise of a transistor and its output power are closely related to its bias current and the power budget of the circuit. Similar to power amplifiers, the output power is a portion of dc power. Therefore, based on the desired output power and/or noise performance of the amplifier, the bias current is selected and then the transistor size can be found from Fig. 4.9 such that the transistor be in its most active (optimum) condition.

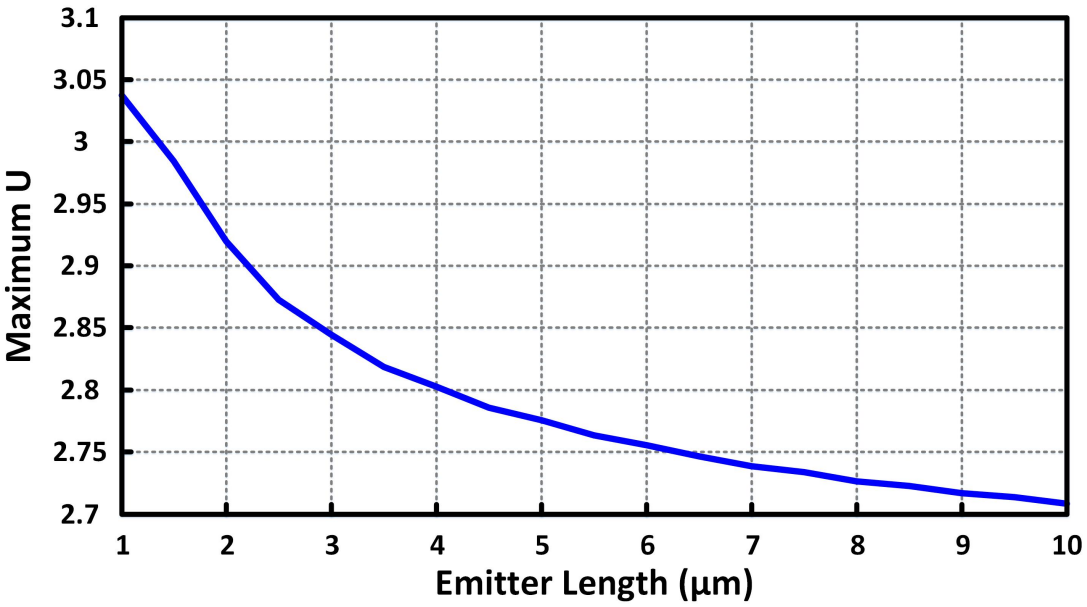

Figure 4.8: Maximum U at 180 GHz for different total emitter lengths (one finger) in a 130 nm process.

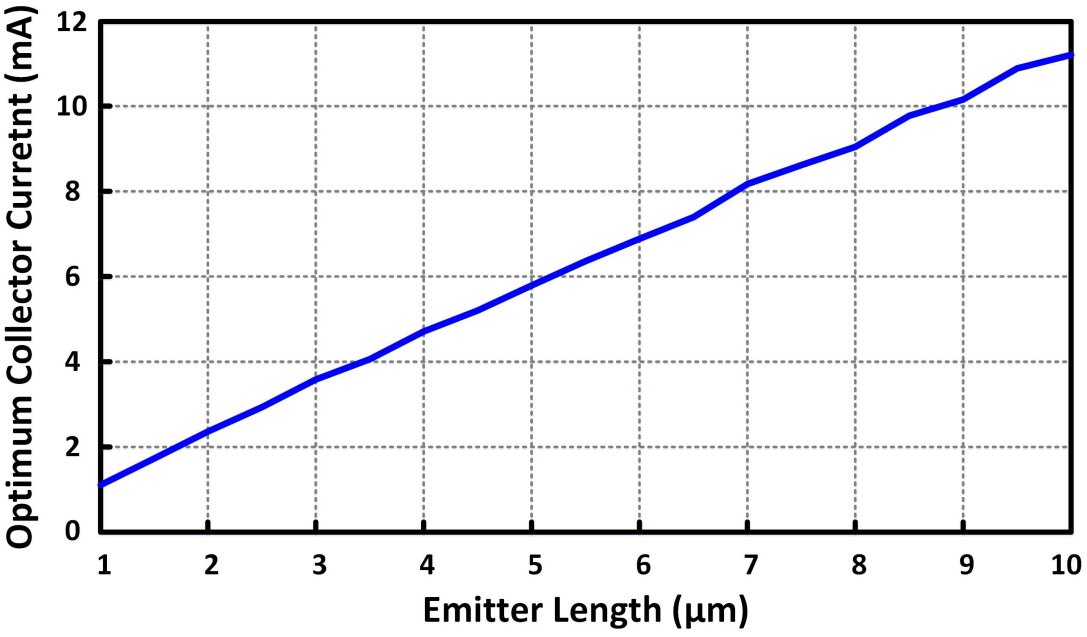

Figure 4.9: Collector current at which U becomes maximum for different total emitter lengths (one finger) at 180 GHz in a 130 nm process

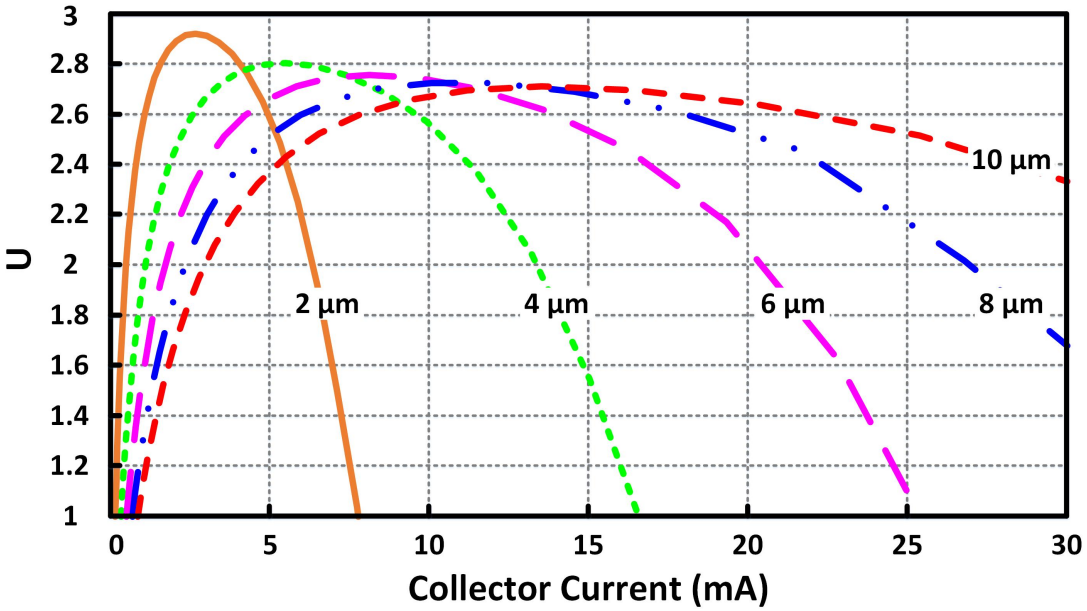

Figure 4.10: U vs. I_c for different total emitter lengths (one finger) at 180 GHz in a 130 nm process

For the sake of completeness, the evolution of a transistor in the gain plane with bias current is shown in Fig. 4.11. For a selected emitter length (selected size from Fig. 4.9), changing the number of emitter fingers, slightly changes the parasitics of the transistor and hence affects the U moderately. Depending on the desired frequency and the selected structure for the embedding, larger C_μ might help/hurt the feedback which is supposed to partially resonate C_μ out. In this work, based on all these considerations and trade-offs, the transistor is chosen to have a total emitter length of 4.2 μm. After choosing the total emitter length, the number of fingers is chosen such that the highest U is achieved. This results in selecting a transistor with $3 \times 1.4\mu$m emitter length. Fig. 4.12 shows G_C and G_{msg} of this device at the selected bias current. As mentioned in the abstract, a three stage amplifier employing this device results in 6.8 dB power gain at 180 GHz assuming perfect conjugate match (see Fig. 4.12).

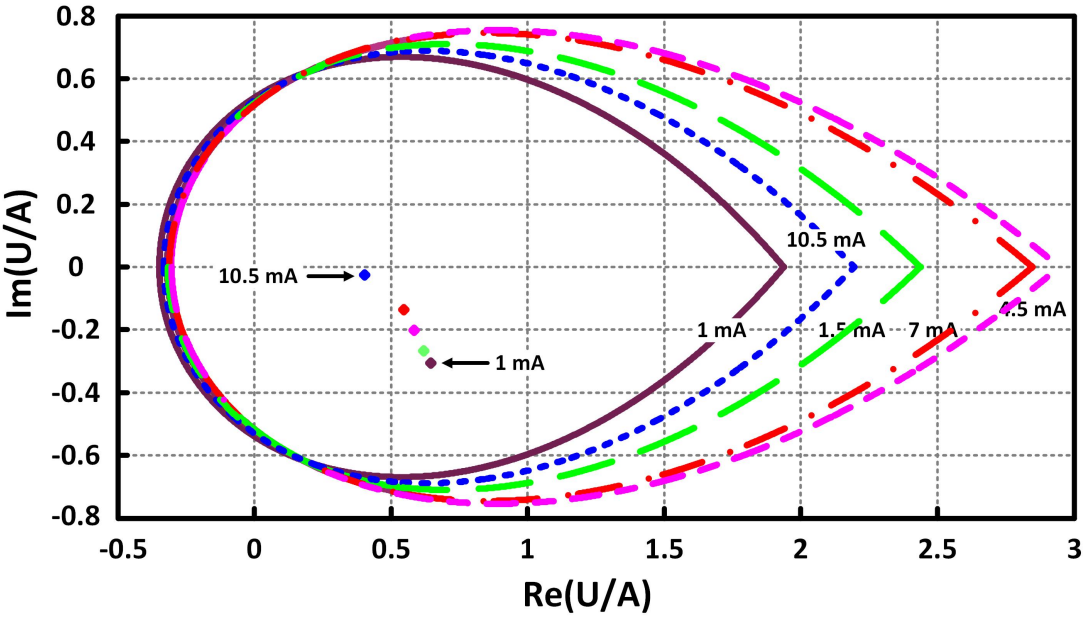

Figure 4.11: Evolution of a transistor with emitter length of $3 \times 1.4\mu$m as bias current increases from 1 mA to 10 mA at 180 GHz in a 130 nm process

4.4.2 Step II: Passive Components Considerations

As the next step, the structure of the passive components should be defined.

Primary optimization using ideal components for the embedding circuit shows that in order to be able to move the employed transistor to the left of the gain plane, Y_b, Y_c and Y_f have to be inductive and Y_e needs to be capacitive. This result is transistors/processes dependent and has to be found either by intuition or by optimization using ideal components.

Remark : It is worth mentioning that since Y_f and Y_b are distributed components, they are not interchangeable in Fig. 4.7, and because of this, this structure provides adequate degrees of freedom for the embedding.

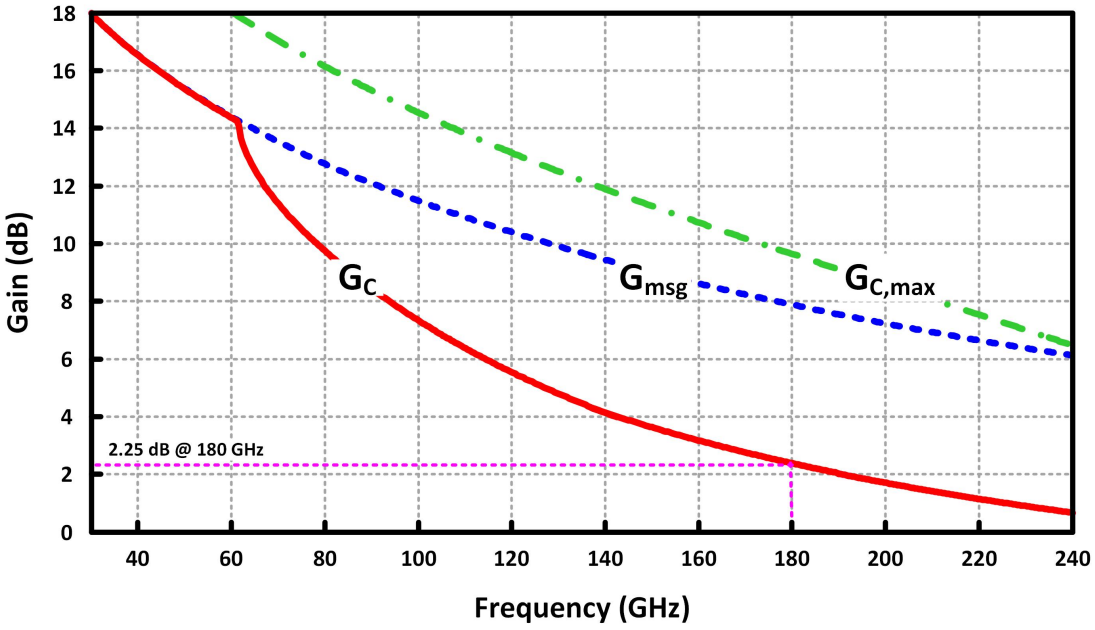

Figure 4.12: G_C, G_{msg} and $G_{C,max}$ of the selected $3 \times 1.4\mu$m transistor biased at optimum collector current in a 130 nm process vs. frequency

4.4.2.1 Transmission Lines

The transmission lines Y_c, Y_f and Y_b are realized as grounded coplanar wave guides (GCPW). This structure provides decent shielding at high frequencies [59] as well as a low-loss return path. The patterned ground plane of the GCPW's is composed of stacked three lower metal layers to provide adequate thickness for reducing the loss (while not being too close to the signal track). It is patterned to decrease the formation of Eddy current loops so that the inductance and thence the characteristic impedance of the line (Z_0) be preserved in the presence of the ground plane. In order to have high quality (low loss) transmission lines, α/Z_0 of the line should be minimized [59] (α is the real part of the propagation constant ($\gamma = \alpha + j\beta$)). This can be studied in HFSS using Optimetrics tool. Intuitively, assume that the distance between the walls is larger than the distance between the signal track and the ground plane. This is a

reasonable assumption since the distance in the latter is usually less than a couple of micrometers. Hence, due to proximity of the ground plane and also the skin effect, most of the current flows on the bottom surface and less on the side walls of the signal track. Therefore, further increasing the distance of the walls from the signal track does not affect the current distribution significantly and thence the loss (α). However, increasing the distance between the walls improves the Z_0 at first and soon saturates and is not worth the area after a certain distance. Thus, the distance between the walls is usually selected based on the area availability. On the contrary, the width of the signal track significantly affects both Z_0 and α. The narrower the track width, the larger both Z_0 and α. Thus, for a given wall distance there is a track width at which α/Z_0 becomes minimum for the desired operation frequency. The thickness of the walls can simply be chosen a couple of micrometers since this way it would be much thicker than the ground plane and usually much farther than that and hence accommodates less return current. Therefore, its conductance has a minor effect on the quality factor of the transmission line. Here,for the operation frequency of 180 GHz, the walls are chosen to be 5 μm thick, the width of the signal track is 3 μm and the inner distance between the walls is 40 μm.

4.4.2.2 Capacitor at Emitter

Y_e is a capacitor with one node connected to the emitter and the other one grounded. Therefore, we need a choke (a quarter wave length transmission line) for bias current. To decrease the energy loss by radiation and also to avoid signal coupling to the substrate and to the rest of the circuit, one plate of C_e is realized as a box in first and third metal layers (connected in three edges, using vias) and the other plate which goes in between, is on the second metal layer connected to the emitter. Since the connecting track is very

short, the resonance frequency of this capacitor is very high and hence its quality factor is very high even though it is fabricated in lower thin metal layers. The choke is realized as a quarter wavelength GCPW transmission line. According to the EM simulations, the quality factor of the combination of the choke and the capacitor is around 20 at the desired frequency. This grounded capacitor which is made using first three metal layers along with the choke can be simply modeled by an ideal capacitor in parallel to a resistor.

4.4.2.3 Decoupling Capacitor

The decoupling capacitor (C_{dcpl}) is not part of the optimized circuit, because primarily it is used to decouple the dc voltages of collector and base and ideally it has to be large enough in order not to affect the impedance of the inductive feedback. However, to have a reasonable size and avoid poor quality factor and large parasitics to the ground (which degrade U), it cannot be very large. Moreover, there is another advantage not to have a very large C_{dcpl} that is not short circuit at the desired frequency. In this case, the transmission lines Y_f and Y_b need to be longer to be able to resonate out this capacitor. This makes these two transmission lines more practical for fabrication at this frequency range. The longer the transmission lines, the lower the proportional variations and modeling errors. Here, C_{dcpl} is designed as a finger capacitor in two top metal layers.

All passives are modeled using HFSS and hence their models include all losses and non-idealities. The final structure has to be EM simulated as a whole to verify that the resultant network has the same expected mapping into the gain plane.

4.4.3 Step III: Optimization

Having the *y*-parameters of the network, the optimum value of the embeddings should be found. Using parametric analysis tool in Cadence it is possible to find an embedding which shifts the network close to the point of G_{Cmax} (the farthest left point on the stability boundary) to get the highest possible gain from the employed transistor. However, the resultant circuit is usually so sensitive to the variations and modeling errors of each component such that a very small deviation from the desired values results in a huge shift in the gain plane, which leads to either instability or low power gain. This indicates that finding an FPLLR embedding to move the network to the high gain stable regions is a very unreliable design method using Cadence parametric analysis tool. Even forgetting about the sensitivity, which is not an option, finding an embedding with four independent components in a reasonable range, requires a huge number of steps which makes it almost impossible to be done in any circuit design tool such as Cadence and ADS.

In fact, we need a method which is capable of finding the embedding while it considers the variations and modeling errors *"during the design process"*, to guarantee that even if the worst case happens, the network remains stable and provides a decent power gain. That is, the corners must not be considered after the design is done merely to perform an analysis to see how they affect the performance of the circuit. We need to take into account all corners in the design stage to make sure that all of them will perform.

In general, a constrained optimization solver can optimize the power gain, while the desired constraints are satisfied. It provides the possibility to maximize the minimum power gain of all considered corners while all of them remain inside the stability region. Similar to the corner analysis, we can assume a typical, a min and a max model for each component to find the circuit corners. For instance, assume that the embedding is composed of one capacitor (with two corners and one typical model) and a transistor which

has typical, bmin and bmax corners. In this case we can think of nine different corners for the whole network. However, usually the extreme cases cover all possibilities such that we need to consider only four corners composed of the combination of the extreme cases of transistor and capacitor. We always take into account the typical case as a reference, and hence we will have four corners and one nominal circuit for this example. Next, we need to find the capacitor such that the power gain of the corner with minimum gain (which is unknown in each iteration before calculating the gain of all corners) is maximized, while all five circuits remain stable. We can also add a margin not to let any of the corners get very close to the stability boundary. However, it is not necessary since all reasonable variations and modeling errors are already included in the corners and we do not expect more change in the fabricated circuit if the considered corners are adequately reasonable. In general if there are n components with foreseeable errors and variations within a reasonable range, there would be 2^n corners and one typical network that all must remain stable while the embedding is chosen such that the gain of the corner with minimum gain is maximized.

The mentioned optimization problem is a constrained polytopic problem [61, 85] maximizing the minimum power gain among all considered corners over the convex stability set.

Given the decoupling capacitor and the biased transistor, the high gain amplifier design can be formulated as follows:

$$\max_{\boldsymbol{Y_f},\boldsymbol{Y_b},\boldsymbol{Y_c},\boldsymbol{Y_e}} \{\min_{i} \boldsymbol{k_i}\}$$

such that:

$$\frac{U_i}{A_i} \in \text{Convex Stability Region in (4.15)}$$

$$i = 1, \ldots, 17,$$

where

$$k_i = \frac{G_{Ci}}{U_i}.$$

Such a problem can be solved using an appropriate constrained optimization solver. Implementing the above problem in a code is simple but the problem itself is quite nonlinear and the original functions of MATLAB such as `fmincon` cannot solve it easily and efficiently. Efficient practical techniques [62] are exploited to simplify the problem for the solvers. A MATLAB code is developed which employs Sparse Nonlinear Optimizer (SNOPT) [60] in order to find the best embedding composed of the transmission lines and capacitors which are modeled using HFSS. A complete table of the y-parameters of each passive components in a reasonable range of values should be provided to the code so that it can find the optimum embedding. It is simple to use a regression method to find the intermediate values if the steps are adequately fine. For instance, considering the fabrication accuracy, it is sufficient to provide the y-parameters of the transmission lines in steps of 5 μm up to half the wave length at the desired frequency.

The results show that instead of shifting the whole circuit towards the far left point on the real axis inside the stability region (i.e. towards G_{Cmax}), the solver has pushed all corners to another spot close to the left side of the region in order to accommodate all corners inside the stability region. As depicted in Fig. 4.13 the corners might be far from each other in the gain plane. This means we would fail to find the embedding by moving

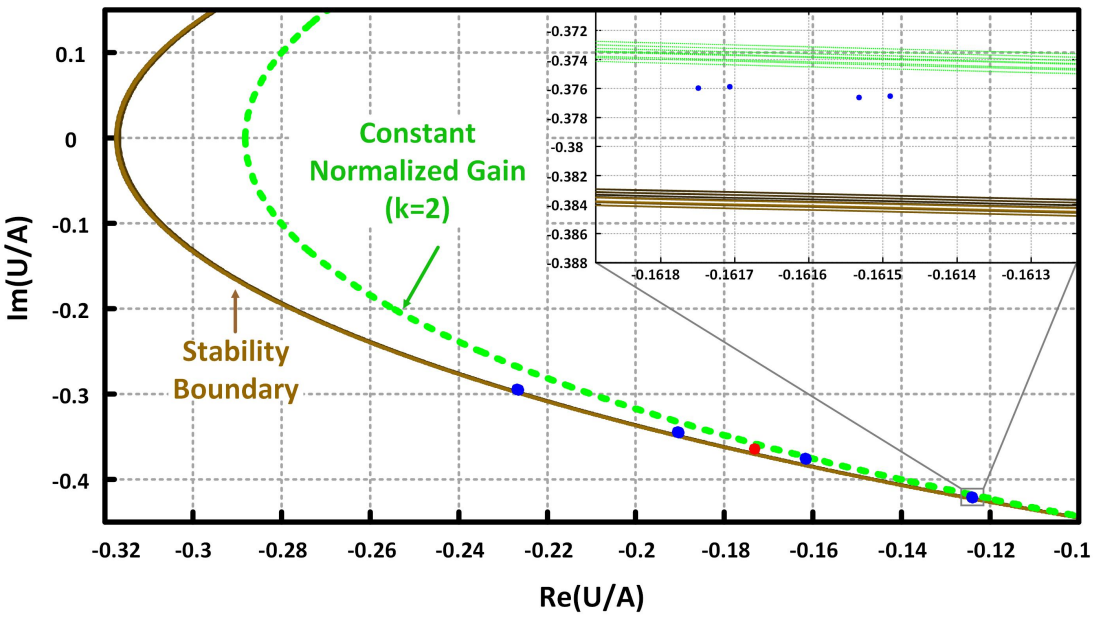

Figure 4.13: Optimized Design where all corners are stable and the minimum normalized gain is more than 2. *Red*: nominal circuit, *Blue*: 16 corners, *Solid Brown:* 16 stability boundaries for different corners (which are slightly different since U is different for each corner because of different losses), *Dashed Green:* loci of normalized gain $k = 2$ for all corners; any point on the left side of these green circles and inside the stability region has a power gain larger than $2 \times U$.

the nominal circuit towards the high normalized power gain regions without knowing the sensitivity of the circuit with respect to each component and how the corners might move in the gain plane away from the nominal network. This complicated problem is efficiently solved by SNOPT.

Remark 1: The advantage of using the proposed stability region in the optimization problem instead of the traditional stability factors such as $k_f - \Delta$ is that it forms a convex constraint which helps the solver to handle the problem very efficiently. Besides, as already mentioned, mapping the network into the gain plane, provides a good understanding about how close to instability we are, and also how close to the maximum theoretical gain the network is. Furthermore, it is a intuitive and graphical way of

understanding gain and stability of a two-port network.

Remark 2: Fig. 4.13 clearly shows that if the stability boundary for large U which intercepts x-axis at -0.25 was used for the design, then the gain would definitely be lower than $2 \times U$ since the gain loci with $k = 2$ intercepts x-axis at -0.29.

4.4.4 Step IV: Input, Output and Interstage Matching

Matching networks are necessary at the input, output and between the stages in order to enhance the power flow and avoid power reflection and loss. There are two main issues regarding the matching circuits at high frequencies.

First, the coupling between the structures becomes very important at high frequency and might degrade the matching performance severely if it is designed separately. Therefore, matching networks have to be EM simulated with the rest of the circuit which makes its design difficult and time consuming.

Secondly, because of the considerable loss in the matching network, particularly due to skin effect at high frequencies, bilateral conjugate-matching is theoretically impossible. Namely, in Fig. 4.14, if $Z_s = Z_{in}^*$ and the matching network is lossless, then Z'_{in} would be equal to 50Ω. However, because of the loss in the matching network, $Z_s = Z_{in}^*$ does not imply $Z'_{in} = 50\Omega$. Hence, it is possible to choose either to have $Z'_{in} = 50\Omega$ or $Z_s = Z_{in}^*$ or we have to find something in between. Therefore, designing a matching network is a challenging problem at high frequencies and in particular, interstage matching is more difficult and if not handled delicately, it can degrade the performance of the circuit drastically.

Here, all matching networks are composed of a piece of GCPW transmission line

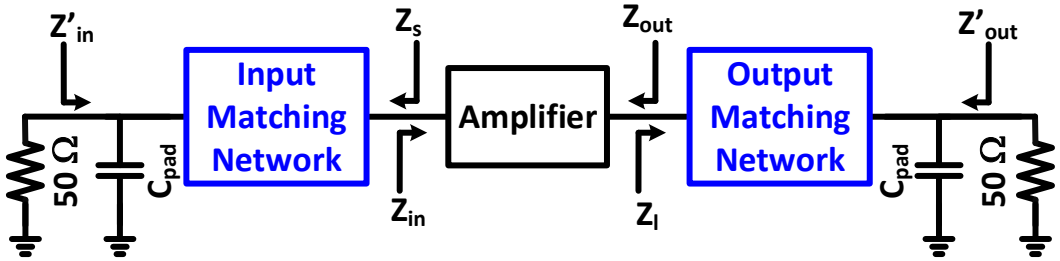

Figure 4.14: Lossy matching network provides unilateral conjugate matching instead of bilateral conjugate matching that a lossless matching network provides. Namely, either $Z_s = Z_{in}^*$ or $Z'_{in} = 50\Omega$.

and possibly a capacitor at each end. Capacitors must be connected to the top metal (to the signal track) and hence there are a set of lossy and inductive vias that connect them together. The distance of the top metal to the bottom metal in the employed process is around 10 μm which is long enough to degrade the quality factor of the employed capacitors at 180 GHz by decreasing its self-resonance frequency and by its loss. Fig. 4.15 demonstrates the input/output and interstage matching traces on the Smith chart for performing complex conjugate matching.

4.4.5 Design Example: A Three-Stage Amplifier

Based on the above proposed method, an three-stage amplifier is designed in this part. At first a one-stage amplifier is designed. Using interstage matching networks, a three-stage amplifier is built upon this one-stage optimized amplifier. As already mentioned, the circuit of Fig. 4.7 is employed to provide enough degrees of freedom for the embedding to be able to move the network to the desired region of the stability set in the gain plane.

In order to have a robust design, all worst case scenarios must be taken into account.

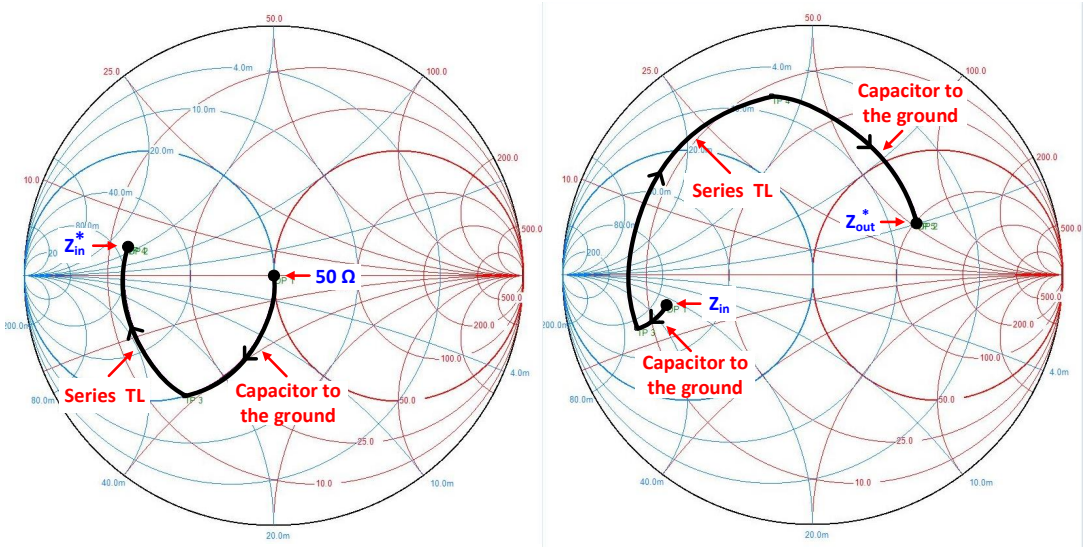

Figure 4.15: Input and interstage matching traces on Smith chart for conjugate matching. The output matching trace is similar to that of input, both start from 50 Ω and move toward the complex conjugate of the input/output impedance.

We assumed that the passive components if large, bear ±5% variation and if small (e.g. Y_b and Y_c usually) bear up to ±15% of error and/or variation. These errors are considered to cover any possible deviation from the typical design, inter-die and intra-die, temperature variations, modeling errors and etc.

In order to attain a reasonable power gain considering all losses, variations and modeling errors, it is preferred not to go beyond $\frac{2}{3}f_{max}$ where U is approximately $(3/2)^2 \simeq 3.5$ dB and the $G_{Cmax} \simeq 8.3$ dB. The f_{max} of the employed 130 nm BiCMOS process is ~280 GHz [55]. Therefore, we design an amplifier around $\frac{2}{3}f_{max} \simeq 180$ GHz in order to achieve a reasonable gain.

Providing the y-parameters of each component and the selected transistor at its desired bias point the optimization problem is solved which finds the length of the transmission lines and the capacitance of C_e. To simplify the problem and decrease the num-

Table 4.1: Optimization results

Component	**Value**
Y_b: Transmission line	Length = 24.1724 μ m
Y_c: Transmission line	Length = 5 μ m
Y_f: Transmission line	Length = 196.649 μ m
Y_e: Capacitor	Capacitance = 28.7537 fF

ber of variables, the variation/error of the transistor, Y_e and Y_c are combined all together and Y_f, Y_b and C_{dcpl} each has separate corners. This way, there exists 16 corners which are the worst cases and also one nominal/typical network. Among all these networks, the code maximizes the minimum normalized gain while constrained by the stability of all 17 corners. For the selected transistor, bias and frequency, the solver has come up with the values shown in Table 4.1, which results in the worst case normalized gain of $k = 2.03197$.

The mapping of the nominal circuit and also those of 16 corners are shown in Fig. 4.16. For each corner, U is slightly different (because of different losses) and so are the stability regions and the constant gain loci.

The complete schematic of the three stage amplifier is shown in Fig. 4.17 along with its die photo which is fabricated in 130 nm SiGe process of STMicroelectronics. The whole passive structure including stacked vias to the base, emitter and collector, the transmission lines, capacitors and also dc and signal pads are carefully Em simulated using HFSS, in order to capture the layout parasitics and all the couplings. The simulated G_T, G_{msg} and $G_{C,max}$ of the designed three stage amplifier are shown in Fig. 4.18. It is worth mentioning that by considering errors and variations in each component in the design level, i.e. during the optimization, the imperfections in the layout such as a

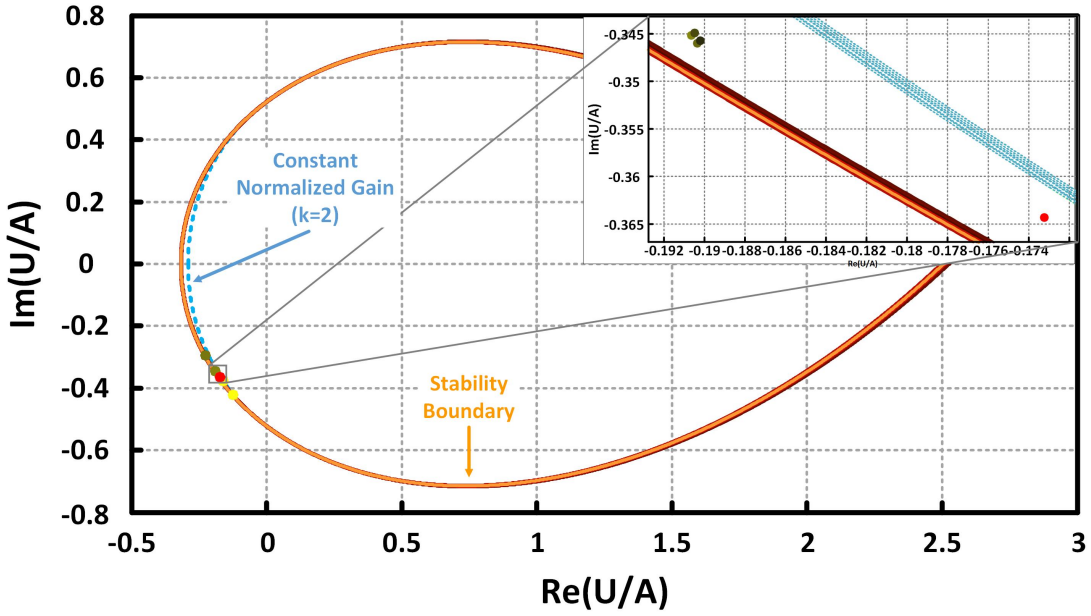

Figure 4.16: Solid lines: Stability boundaries for all corners and nominal circuit, Dashed lines: Loci of normalized power gain $k = 2$ for all corners and nominal circuit. Dots: The nominal circuit and 16 corners on the gain plane

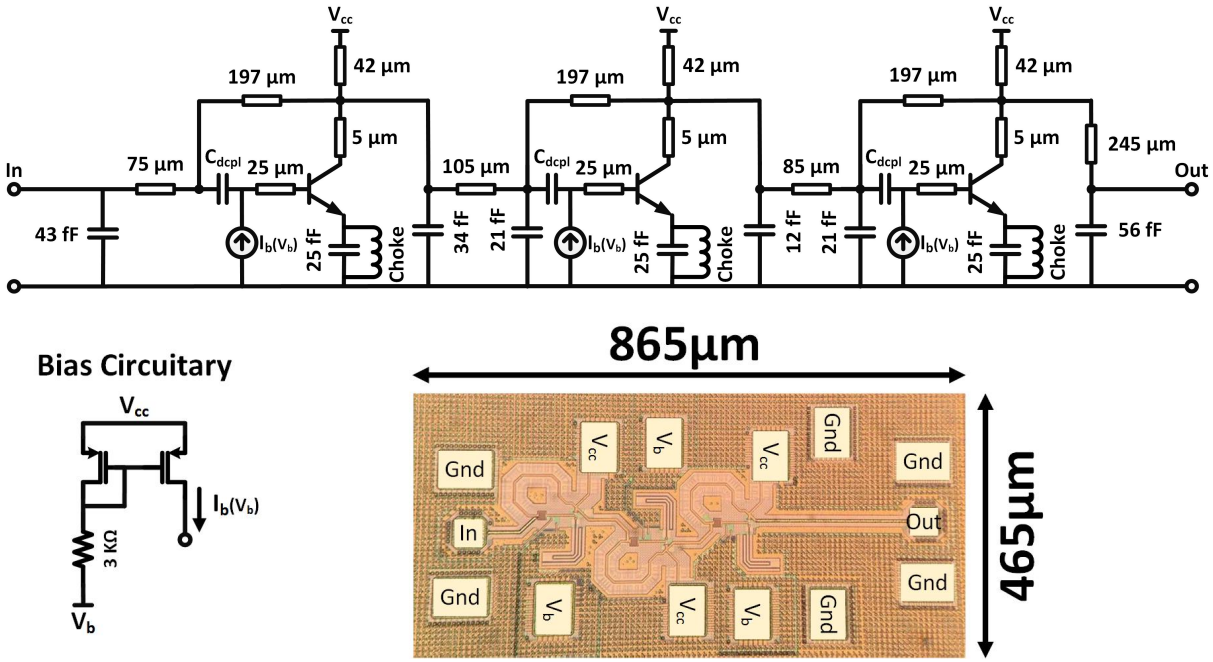

Figure 4.17: Three-stage amplifier schematic and die photo

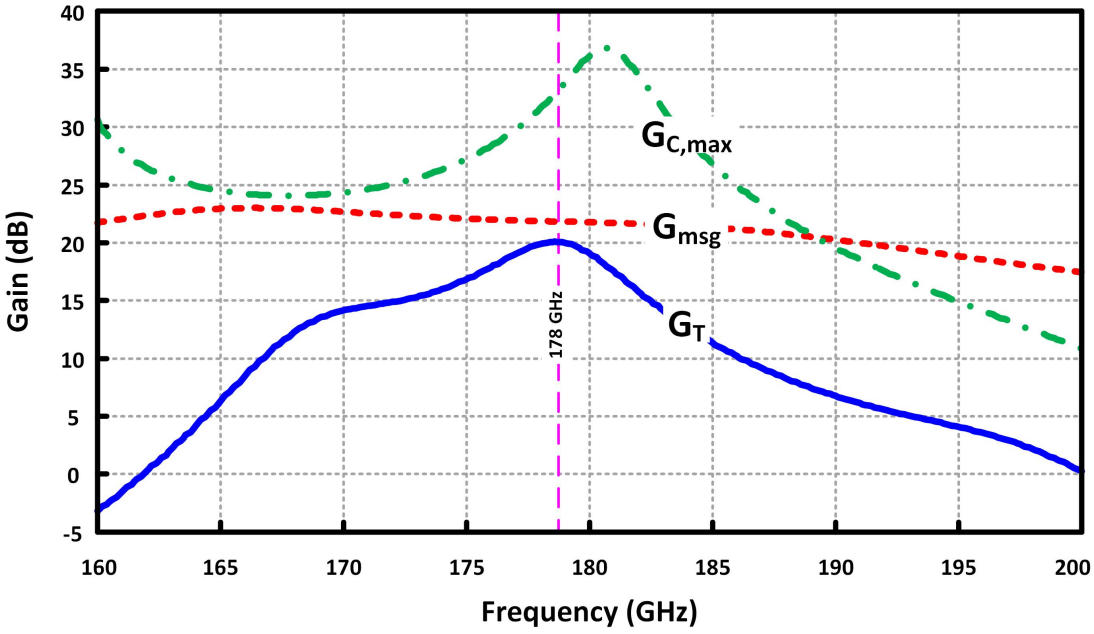

Figure 4.18: simulated G_T, G_{msg} and $G_{C,max}$ of the three stage amplifier in a 130 nm process.

bending GCPW whose model slightly deviates from the straight one, would not affect the performance of the resulting amplifier significantly.

4.5 Measurement Results

The employed setup for measuring the S-parameters is depicted in Fig. 4.19. A 67 GHz PNA-X is used along with VDI WR5.1 extenders which are connected to two Cascade I-220 GSG probes via WR5.1 S-bends. The whole measurement setup is calibrated up to the probe heads with minimum possible input power level in order to measure the small signal S-parameters.

The measured S-parameters are shown in Fig. 4.20 along with the simulation results.

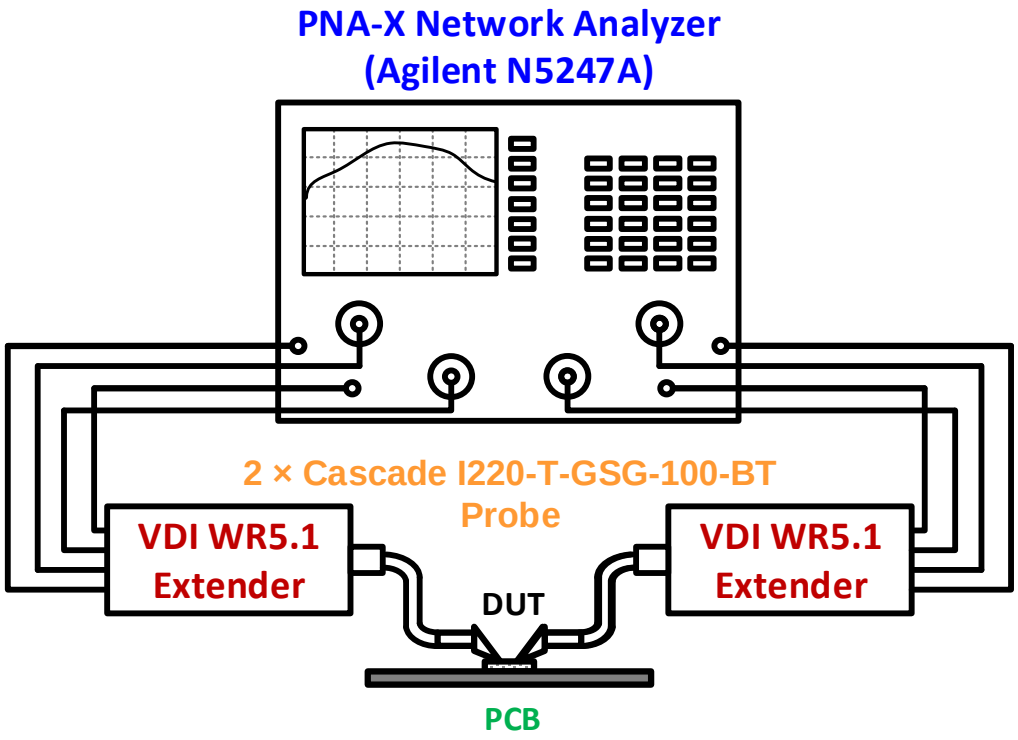

Figure 4.19: S-parameters measurement setup

The measured results show a reasonable 8.2 GHz 3 dB band width and a power gain of 18.5 dB at 173 GHz while consuming 42 mW dc power from 1.8 V supply. The measured stability factor is shown in Fig. 4.21 which indicates that the amplifier is stable.

Fig. 4.22 demonstrates the setup which has been used to measure the large signal behavior of the amplifier. The input power is swept using PNA while the output power is measured using VDI Erickson PM4 power meter. The saturated output power is 0.9 dBm. The results are shown in Fig. 4.23.

Table 4.2 compares the results of the state of the art methods and that of this work.

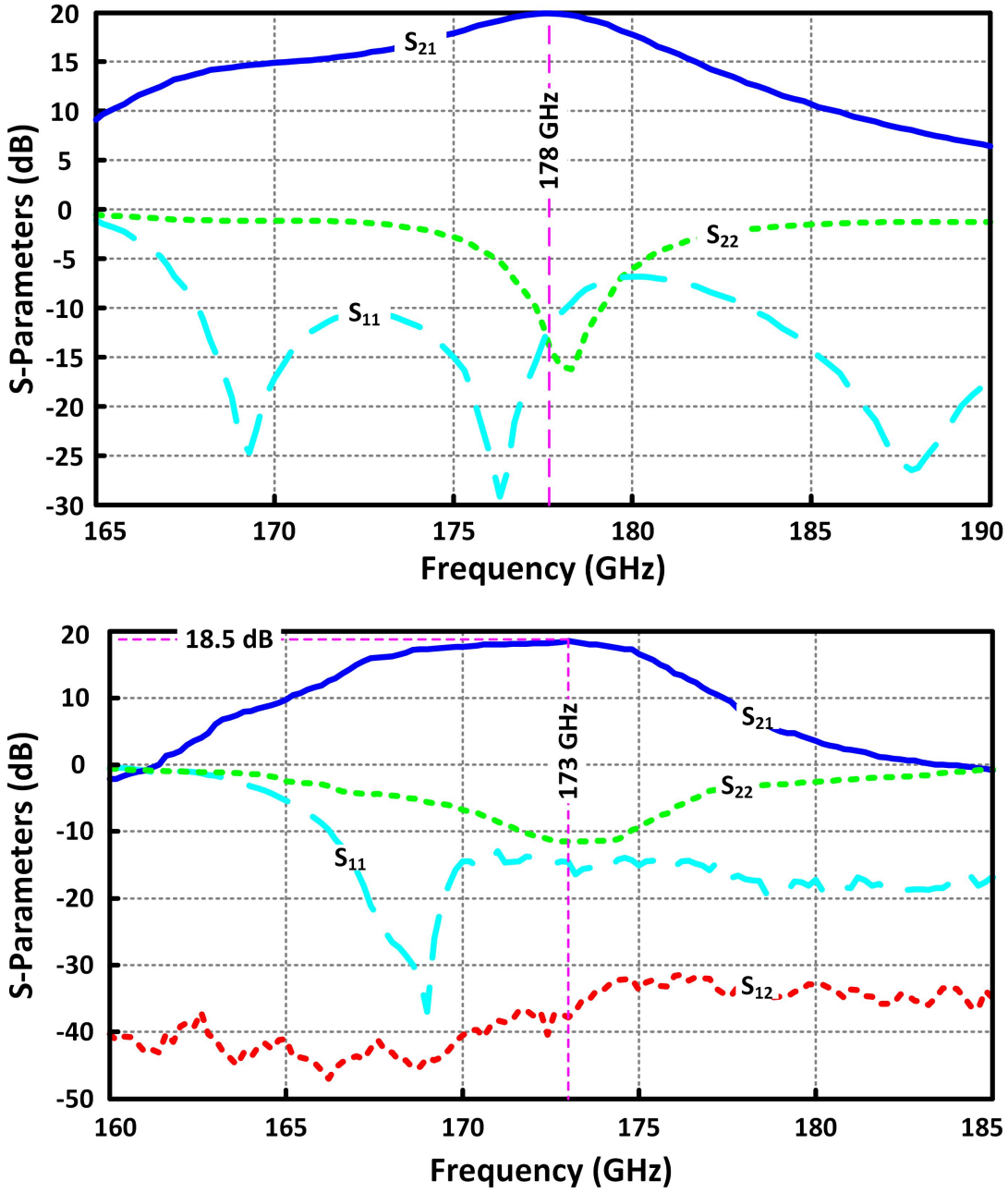

Figure 4.20: The S-parameters of the designed three stage amplifier, Top: simulated, Bottom: measured

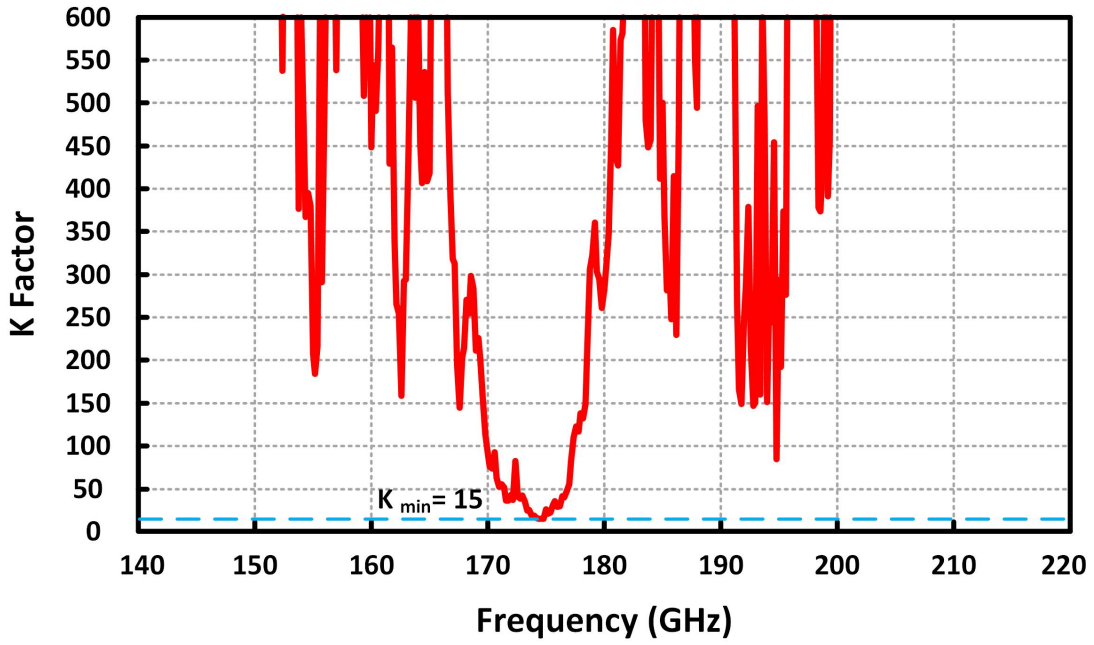

Figure 4.21: The measured stability factor of the amplifier

As already mentioned, the maximum power gain that a device can provide is directly related to its unilateral power gain independent of the frequency or the employed process. Hence, to be able to compare different methods independent of the employed processes, the normalized power gain of each stage of the resulting amplifiers must be compared. The FoM is defined as :

$$FoM = \frac{\sqrt[n]{G_T}}{U(f)}, \tag{4.17}$$

in which n is the number of gain devices and $U(f)$ is the unilateral power gain of the employed device at the operation frequency. This FoM shows how efficient a design procedure extracts the maximum possible gain out of each active device. As shown in Table 4.2, the results of this work clearly prove the effectiveness of the proposed method.

Remark: It is noteworthy that dc power consumption is not directly included in the FoM. As discussed before, maximum power gain of a device is solely related to U (and

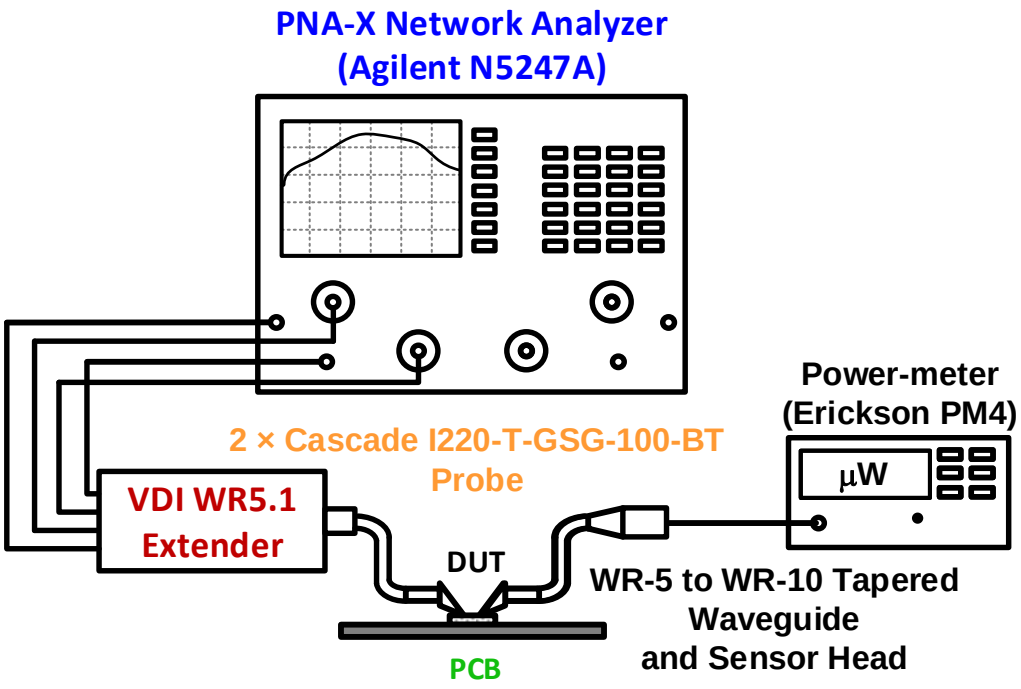

Figure 4.22: Large signal measurement setup

thence to the f_{max} of the process). On the other hand, transistors of different processes achieve their maximum U (at the desired frequency) in different bias currents (and different current densities), i.e. similar dc power consumptions do not result in similar U in different processes. To clarify this point,consider two unilateralized single-stage amplifiers designed in two different processes using ideal passives, both at a frequency where $U = 4$. These two amplifiers will have identical power gain of 4. Since the method is exactly the same and passives are ideal, the FoM should be similar. However, usually these two amplifiers consume different dc powers to result in a power gain equal to the U which means same unilateralization method does not achieve the same FoM in two different processes if dc power consumption is included in the FoM. In other words, dc power would be different while the method and its ability to extract power gain out of

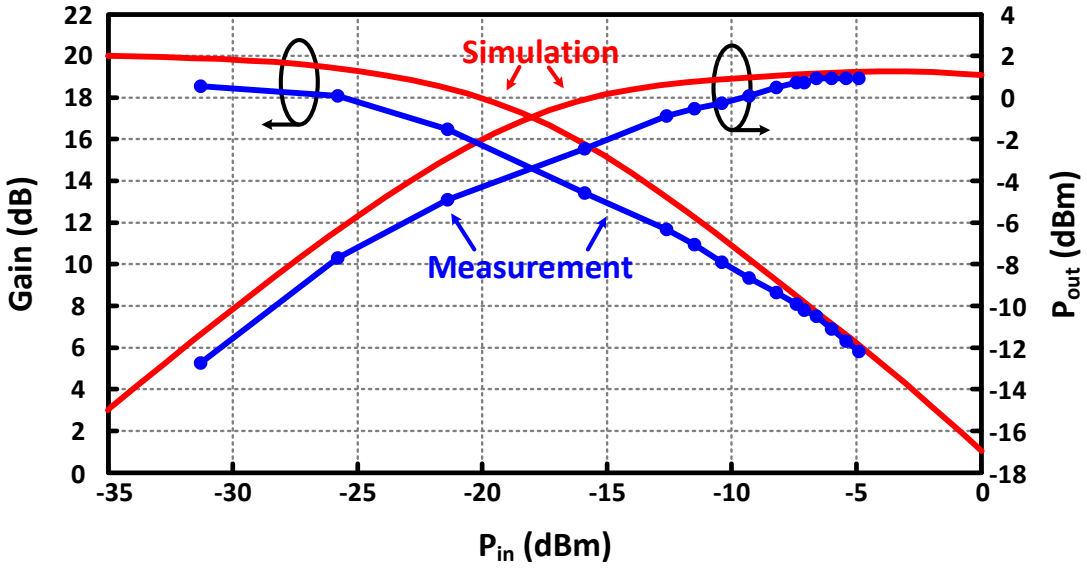

Figure 4.23: Large signal measurement of the output power and gain versus input power

the device is the same, i.e. $G_C/U = 1$ in both cases. This example clarifies that including dc power in the FoM leads to misleading results when considering the efficacy of the method in extracting power gain from the device. In fact, it is not fair to compare two design methods in two different process while one of the process specs (dc power consumption) is playing an important role in determining the FoM. The proposed FoM is defined to fairly compare different amplifier design methods independent of the process and solely by comparing the efficiency of the utilized method in achieving high power gain.

4.6 Conclusion

A novel systematic approach to design high gain amplifiers above $f_{max}/2$ of the utilized transistor is proposed. In order to find the best embedding that can extract the maximum

Table 4.2: Comparison table

	Freq. (GHz)	Gain (dB)	P_{sat} (dBm)	P_{dc} (mW)	f_{max} (GHz)	$U(f)$ (dB)	3 dB BW (GHz)	FoM
[72]	140	8	-1.8	63	240	4.7	10	0.46
[37]	140	18	NA	112	300	6.63	18	0.5
[73]	144	20.6	5.7	54.6	240	4.42	-	0.8
[86]	150	8.2	6.3	25.5	320	6.6	27	0.41
[87]	170	15	> 0	135	340	6	10	0.39
[88]	200	17	> -3.5	18	450	7	44	0.53
[89]	210	15	NA	144	435	6.33	30	0.41
[90]	213	10.5	-3.2	42.3	275	2.21	13	0.79
[79]	233	22.5	NA	68	450	5.72	10	0.51
[80]	257	9.2	-3.9	27.6	350	2.68	12.2	0.86
This work	**173**	**18.5**	**0.9**	**42**	**280**	**4**	**8.2**	**1.65**

possible gain out of the active device, a new stability theory is developed. An optimization solver finds the embedding to maximize the power gain while all considered corners remain inside the developed convex stability region. The resulting three-stage amplifier has the best normalized power gain compared to all previous designs considering the capability of the utilized transistors at the operation frequency.

4.7 Appendix

In order to be able to define the stability constraints and optimizing the power gain, we had to derive many related equations. Here we provide some of those equations we

have derived for the first time. The stability region has a boundary composed of two parabolas:

$$y^2 + x^2 = 2Ux - 2U^2\sqrt{\frac{U^3 - 2Ux + 2x - U}{U^3}} - 2U^2x - U^2 + 2U^4 \tag{4.18}$$

where $x = Re(U/A)$ and $y = Im(U/A)$. The closed convex stability region intercepts x-axis at $x = U$ and

$$x = U + 2\sqrt{U^4 - U^3} - 2U^2 \leq -0.25.$$

It intercepts vertical axis at

$$y = \pm\sqrt{2U^3\sqrt{U^2 - 1} - U^2 + 2U^4}$$

which approaches to ± 0.5 as $U \to \infty$. As $U \to \infty$, the stability region becomes:

$$y^2 \leq x + 0.25, \tag{4.19}$$

which is a parabola open towards the positive horizontal axis and intercepts the x-axis only at -0.25 and y-axis at ± 0.5.

The constant gain loci are the following circles:

$$(k^2 - \frac{k}{U^2})y^2 = k(1 - \frac{x}{U})^2 - (1 - kx)^2, \tag{4.20}$$

on which $G_C = kU$. The centers of the circles are at

$$(x = \frac{U^2 - U}{kU^2 - 1}, y = 0),$$

and their radii are:

$$R = \frac{\sqrt{k + \frac{1}{kU^2} - \frac{2}{U}}}{k - \frac{1}{U^2}}.$$

These loci intercept the stability boundary at:

$$x = \frac{(kU)^2 - 2kU^2 + 1}{2k^2U - 2(kU)^2},$$

and the horizontal axis at:

$$\frac{U(1 \pm \sqrt{k})}{kU \pm \sqrt{k}}.$$

Finally, mapping a two-port network with a unilateral power gain of U to the gain plane by calculating its coordinates ($x = Re(U/A), y = Im(U/A)$), we can find on which gain locus it lies:

$$k = \frac{1 + 2x - \frac{2x}{U} + \frac{x^2+y^2}{U^2} - \sqrt{(1 + 2x - \frac{2x}{U} + \frac{x^2+y^2}{U^2})^2 - 4(x^2 + y^2)}}{2(x^2 + y^2)}, \qquad (4.21)$$

where $G_C = kU$.

CHAPTER 5

A 183 GHZ SINGLE-STAGE AMPLIFIER WITH 9.5 DB POWER GAIN: A NEW APPROACH TO DESIGN HIGH FREQUENCY CASCODE AMPLIFIERS

A novel approach to design a mm-wave high power gain cascode amplifier is proposed. The gain is enhanced by adjusting the size of the cascode transistor together with a desensitized inductive impedance at its base. The impedance at this node has a critical role in determining both gain and stability. The employed desensitization technique decreases the effect of process variations and modeling errors on this impedance which results in a reliable design. Providing enough degrees of freedom, this method results in a conjugate matched input and output impedances. Therefore, two or more of this stage can be simply cascaded to get higher gain with no need for an interstage matching network and hence no additional loss and gain degradation. Based on this approach, a single stage amplifier at 183 GHz is implemented in a 130 nm SiGe process which has a power gain of 9.5 dB, 3 dB bandwidth of 8.5 GHz and saturation power of -2.8 dBm.

5.1 Introduction

Myriad applications of mm-wave and terahertz systems [14,16,20–22,25,70] necessitate the design of high gain amplifiers and efficient sources. Amplifiers are one of the basic blocks in many systems. Since generated power in these frequency ranges is usually very small [6], the role of amplifiers becomes more crucial. At high frequencies, the existing transistors are close to their maximum frequency of oscillation (f_{max}). As frequency approaches f_{max}, the activity of the device decreases and thence its ability for power generation [13] and amplification degrades [10]. The degradation of activity can be seen

from the unilateral power gain of the device (U), which is the activity Figure of Merit (FoM) [8]. It decreases by a slope of 20 dB/dec above the $f_{max}/2$ [38], and reaches 0 dB at f_{max}, beyond which the device is no longer capable of power amplification. Moreover, the passive components and metalizations are more lossy (due to both skin effect and operating close to their self-resonance frequency), which results in poor efficiency. This in turn, makes mm-wave design more challenging.

To facilitate and improve the power flow in an amplifier, both input and output ports must be simultaneously conjugate matched (SCM) so that all the available power at source enters the amplifier and the maximum possible power is delivered to the load. The two-port network must be unconditionally stable at the desired frequency to be SCM [82]. There is a trade-off between power gain and stability [57]. However, having poor stability does not necessarily results in a high power gain [7]. Since solid-state circuits are strongly affected by many types of variations, being too close to the stability boundary without considering the potential errors and variations is very risky and might result in an unstable or low-gain fabricated amplifier [7]. Meanwhile, there is a theoretical limit for the maximum power gain of an SCM amplifier (G_C) [10]. The maximum power gain of a stable two-port network at a desired frequency has a straight relation with its unilateral power gain, which is expressed as $G_{Cmax} = (\sqrt{U} + \sqrt{U-1})^2$. This bound demonstrates the vital role of the unilateral power gain as an inherent measure of a two-port network and emphasizes on the fact that capability of a device for power amplification degrades significantly as the frequency passes $f_{max}/2$.

To the best of our knowledge, there are two systematic methods to design high gain mm-wave amplifiers. The first one is the so-called unilateralization [54, 74–79], where the reverse signal path from the output to the input is eliminated. Theoretically, this method results in a stable two-port network with a gain of $G_C = U$. In reality, however,

considering the number of employed active devices, none of the reported works achieve a power gain more than $0.51U$ in measurements [79], which is due to the variations and modeling errors and also the incapability of the proposed methods to design a unilateralized network with lossy passives. The second method is a systematic way to design an optimized passive embedding to achieve a power gain close to the theoretical limit that the device is capable of (G_{Cmax}), and at the same time considers the corners to result in a reliable high gain amplifier [7].

In this work, instead of a passive embedding, an active one is utilized. The new method employs nonidentical cascode device and a desensitized inductive impedance connected to its base to achieve reliable stability and high power gain. This approach provides degrees of freedom which makes it possible to have a fully complex conjugate matched input/output and a high power gain at the same time. A cascode amplifier is very sensitive to the impedance at the base of the cascode transistor which in this case is a very short transmission line. A desensitizing technique is proposed to overcome the modeling errors and variations of such a short transmission line in fabrication.

The rest of this paper is organized as follows. Some basics of two-port networks are reviewed in Section 5.2. A new approach to design a cascode amplifier is proposed in Section 5.3, based on which a high gain single-stage amplifier is designed. Section 5.4 shows the measurement results which prove the efficacy of the proposed method. Finally, Section 5.5 concludes this work.

5.2 Power Gains and Stability

Maximum power gain of an active two-port network is theoretically limited by $G_{C_{max}} = (\sqrt{U} + \sqrt{U-1})^2$ [10] as mentioned above. At low frequencies where U is very large,

this can be approximated by $G_{Cmax} \simeq 4U$ which means G_{Cmax} is 6 dB higher than U. This limit is far from the reach (due to the variations and modeling errors) such that a gain higher than U is very remarkable. Therefore, close to the f_{max}, where the activity of the device is degraded and hence U is small ($U(f_{max}) = 1$), having a high power gain is a hard goal to achieve. One way to improve the power gain is to employ more active devices, either in cascade or cascode structures.

Although an amplifier which is close to instability does not necessarily provide a high power gain, but higher gains always happen close to the stability boundary [7]. Therefore, in an amplifier design process, these two characteristics should be considered simultaneously.

It is shown that a two-port network is unconditionally stable if the following inequalities are all satisfied [10]:

$$g_{11} \geq 0, \tag{5.1}$$

$$g_{22} \geq 0, \tag{5.2}$$

$$2g_{11}g_{22} - M \geq L, \tag{5.3}$$

where $M + jN = y_{12}y_{21}$, $L = |y_{12}y_{21}|$ and $y_{il} = g_{il} + jb_{il}$ are the y-parameters of the network. In most active devices, the first two inequalities are naturally satisfied and potential instability is usually caused by the failure to satisfy the third condition.

Several power gains are defined for a two-port network [10] such as the transducer power gain (G_T):

$$G_T := \frac{P_{Load}}{P_{av,Source}} = \frac{4|y_{21}|^2 g_s g_l}{|(y_{11} + y_s)(y_{22} + y_l) - y_{12}y_{21}|^2}, \tag{5.4}$$

maximum stable power gain (G_{msg}):

$$G_{msg} := |A|, \tag{5.5}$$

where

$$A := y_{21}/y_{12},$$

and unilateral power gain (U):

$$U := \frac{|y_{21} - y_{12}|^2}{4(g_{11}g_{22} - g_{12}g_{21})}. \tag{5.6}$$

G_T is the most useful power gain since matching at both input and output ports are considered [57]. It is equal to G_C in case of SCM, which is compulsory for an amplifier in order to absorb the maximum power from the source and also to deliver the maximum power to the load [7]. U is the activity FoM and is invariant under linear-lossless-reciprocal embedding [8]. It is equal to G_T if the network is unilateral, i.e. $y_{12} = 0$. G_{msg} is equal to G_C at the stability boundary [10].

There is an effective graphical tool, the so-called *gain plane*, that can be effectively employed for designing amplifiers. It is a more suitable compared to Smith chart. In fact, Smith chart studies the effect of load and source impedances (peripherals) on the performance of an amplifier whereas, in the gain plane the most inherent measures of a two-port network as an amplifier are studied [7]. Both power gain and stability of a two-port network can be intuitively and quantitatively studied using this tool. Fig. 5.1 shows the gain plane where the stability boundary along with some of the constant G_C loci are depicted for $U = 3$.

It is straightforward to map a two-port network into the gain plane by calculating the real and imaginary parts of U/A. This mapping simply reveals two important facts about the amplifier. First, it shows if it is stable or not, and also demonstrates how far it is from stability boundary. Second, the network lies on a constant G_C loci which reveals its power gain and more importantly shows how much further gain can be attained from this network by a proper design. To fully utilize a network, it should be shifted toward the

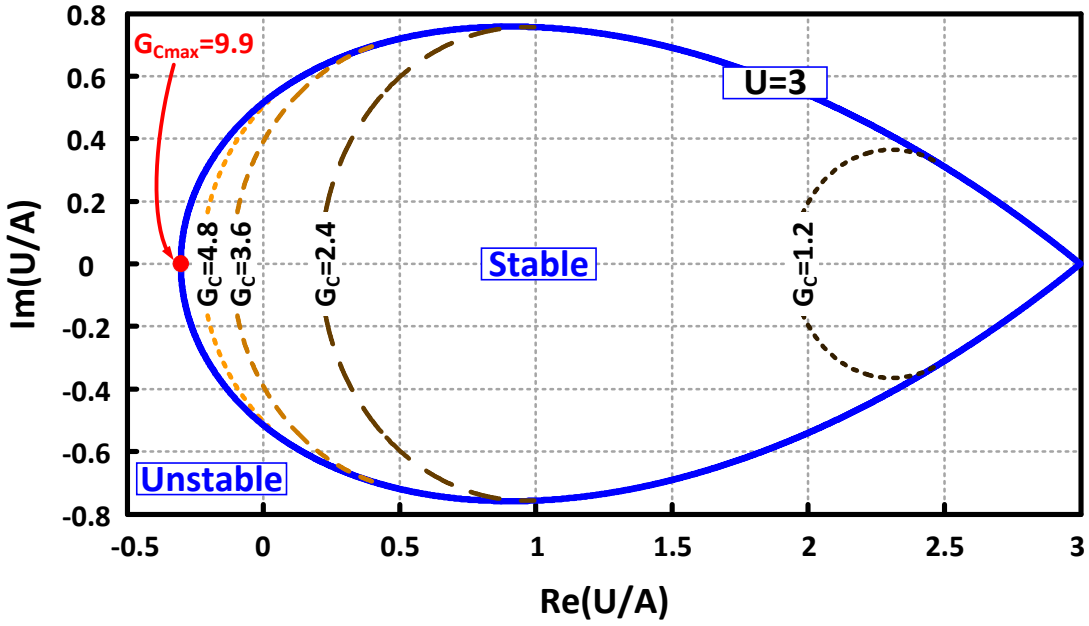

Figure 5.1: *Gain plane*, Solid (blue): Stability region is inside the closed set in the gain plane (for a transistor at $f = 0.6 f_{max}$). Dashed: Constant power gain loci (circles).

left side inside the stability region [7]. This is performed using passive components [7].

5.3 High Frequency Cascode Amplifier Design

In this section, a novel method to design a high power gain cascode amplifier close to f_{max} is presented based on which an amplifier at 180 GHz is designed and implemented.

Traditionally the transistors are chosen to be identical (balanced) in a cascode stage [79, 88]. In this work, using a nonidentical cascode transistor (i.e. designing an unbalanced cascode stage) together with a desensitized inductive impedance connected to its base, the network is brought to the stable high gain regions in the gain plane. That is, in contrary to [7], an active embedding is employed to shift the network to the high gain

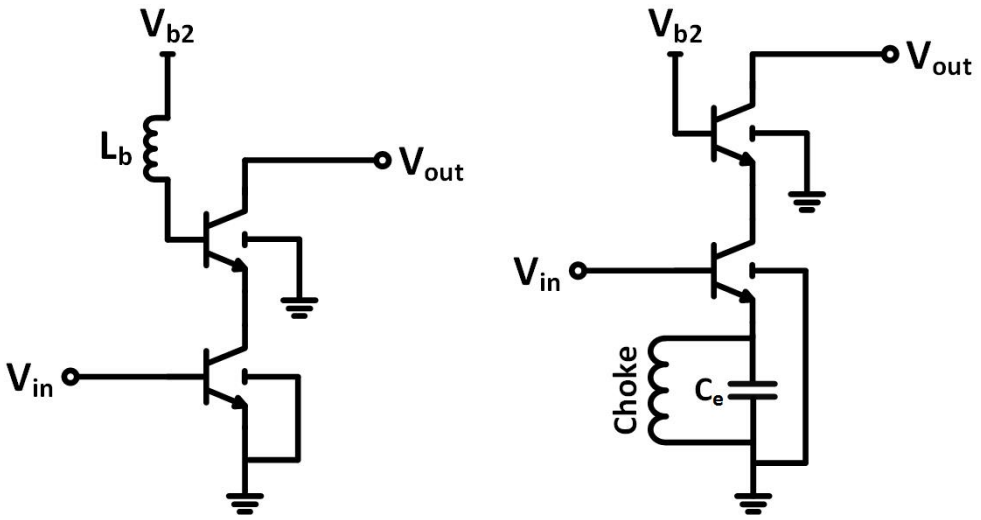

Figure 5.2: There are two possible positive feedbacks in a cascode structure, an inductive one at the base of the cascode transistor and a capacitive one at the emitter of the main transistor.

stable regions.

There are two positive feedbacks that can be employed to enhance the gain of a cascode amplifier. A capacitive impedance in the emitter of the main device or/and an inductive impedance in the base of the cascode device (see Fig. 5.2). The former necessitates use of a choke to provide a path for the bias current. It also decreases the real part of the input admittance which may violate the first inequality in (5.3) if it is not designed properly. The latter suffers only from causing a similar problem in the real part of the output admittance. Comparably, adding the inductive impedance at the base of the cascode device should be handled properly not to result in violation of the second inequality of (5.3). Both of these feedbacks encumber the design of a matching network by decreasing the real part of the input/output admittance, respectively.

In a cascode structure, having an inductive impedance at the base of the cascode transistor is unavoidable. The base is at the lower metal layers and has to be connected to the DC pad at the highest metal layer which usually has some horizontal distance too

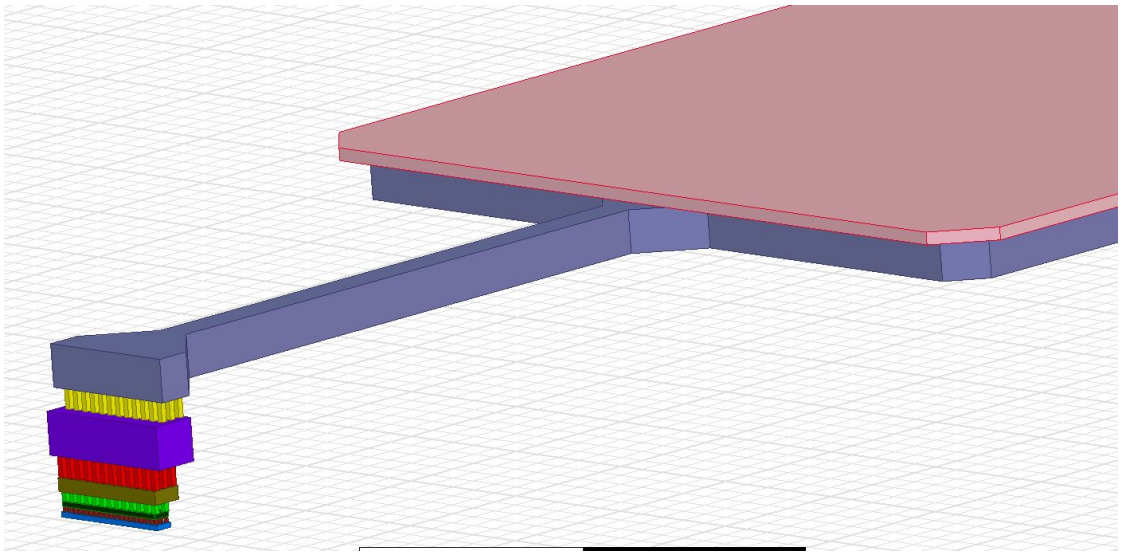

Figure 5.3: Inductive impedance at the base of a cascode transistor is unavoidable since it has to be biased.

(see Fig. 5.3). This connection introduces at least a couple of pH inductance to this node. Hence, in this work the inductive feedback at the base of the cascode device is employed and capacitive feedback is not employed to save the area by eliminating the quarter wavelength choke.

As demonstrated in Fig. 5.4, a conventional cascode stage (balanced cascode) becomes unstable with a small inductance at this node. Moreover, even if it remains stable, a very small change in this impedance significantly affects the gain. That is, the amplifier is very sensitive with respect to this impedance and is not reliable (changing gain from 9.4 dB to 13 dB with only 3 pH increase in the inductance as depicted in Fig. 5.4). Because of this sensitivity, an extra attention must be paid to this impedance.

Modeling errors and process variations of the whole metalization and visa from the base to the DC pad result in a poorly defined inductance at such a sensitive node. Therefore, as the first step in this approach, the inductance of this node has to be increased

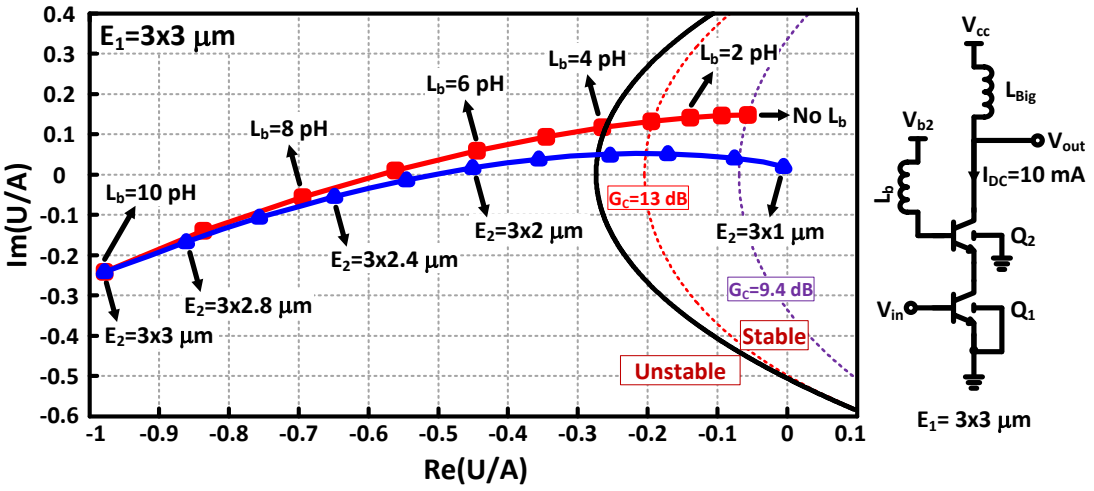

Figure 5.4: Square *(Red)*: small inductance in the base of the cascode transistor of a balanced cascode stage renders the network unstable. Triangle *(Blue)*: an unstable cascode stage with a 10 pH inductance at its base can be stabilized by decreasing the size of the cascode transistor (unbalanced stage).

to have a reasonably accurate and defined impedance. This is done by adding a piece of transmission line (TL) to this node which should be co-designed with the pad. A desensitization technique is employed for implementing this TL to further enhance the robustness of the amplifier.

A short TL is significantly affected by modeling errors and variations whereas a long one is affected negligibly. Thus, in order to desensitize this impedance, the length of the TL should be made longer. The input impedance of a grounded short TL can be approximated by $Z_{in} \simeq jZ_0\beta l$, where l is the length and β is the imaginary part of the propagation constant ($\gamma = \alpha + j\beta$). Hence, to increase the length of the line while the input impedance remains constant, Z_0 should be decreased. To do so, since for a low-loss TL, $Z_0 \simeq \sqrt{L/C}$, the capacitance of the TL should be increased and its inductance has to be decreased. A grounded coplanar wave guide (GCPW) is utilized in this work whose Z_0 is decreased by widening and thickening the signal track and also by bringing

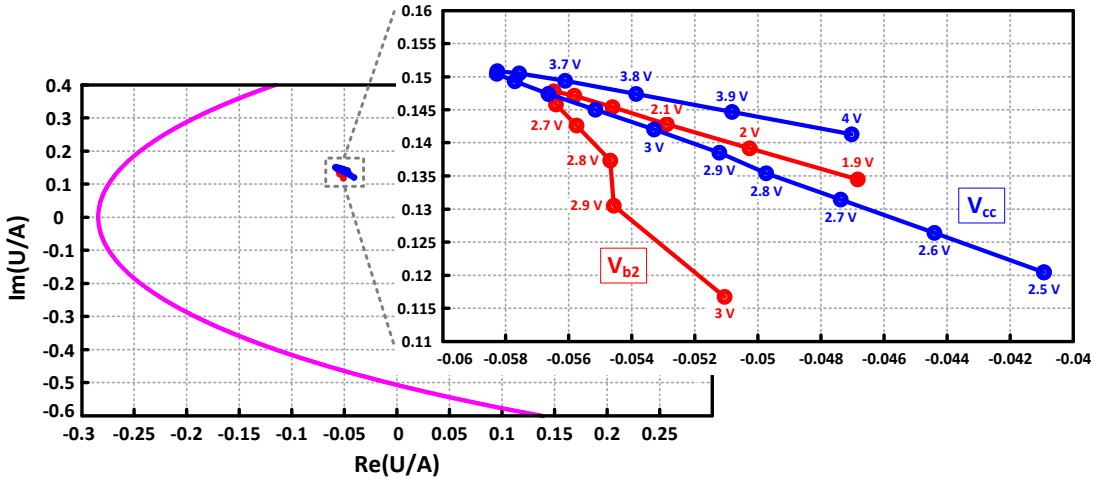

Figure 5.5: The effect of V_{b2} and V_{cc} on the gain and stability is negligible in a reasonable range.

the ground walls nearer to each other and raising the ground plane closer to the signal track.

Next, the size of the cascode device should be properly adjusted to have a stable high gain amplifier. In fact, intentionally increasing the inductive impedance at the base results in an unstable network. This instability can be resolved by appropriate sizing of the cascode device. As shown in Fig. 5.4, decreasing the size of the cascode device, brings back the network to the stability region.

It is worth mentioning that in contrary to the base impedance, the amplifier is not sensitive to the bias base voltage of the cascode transistor (V_{b2}) and the power supply (V_{cc}) as depicted in Fig. 5.5. Hence, it is not possible to move effectively the amplifier in the gain plane by changing these DC voltages. Therefore, stabilization cannot be achieved by adjusting these voltages.

Finally, it is desirable to design a cascode amplifier that can be easily cascaded with itself to provide a higher gain. As can be seen in Fig. 5.6, several pairs of base

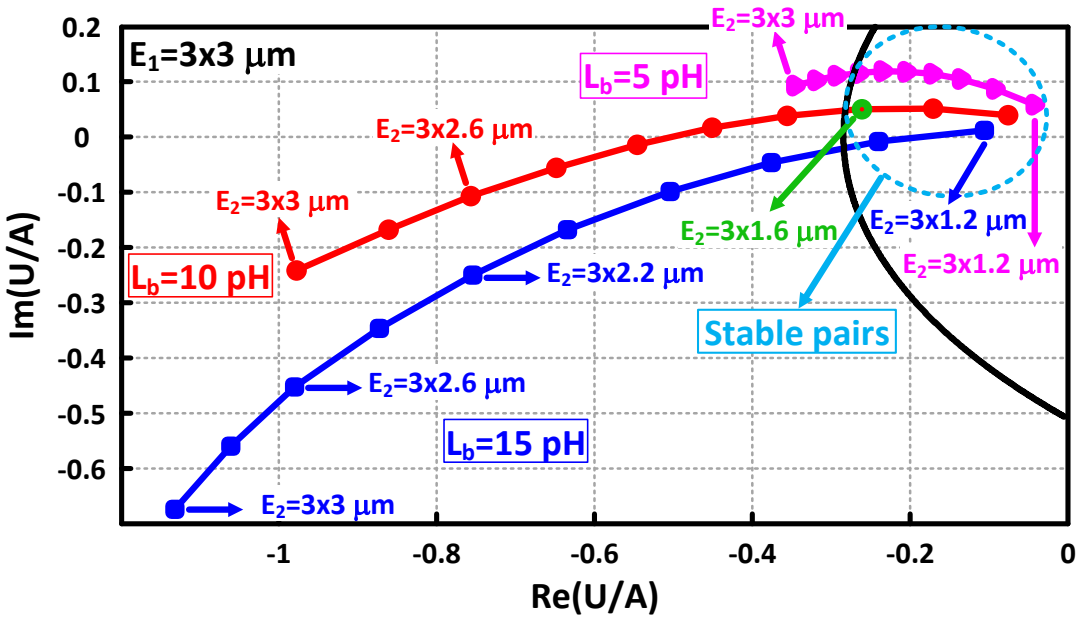

Figure 5.6: Different pairs of inductance and size (of the cascode transistor) can be chosen to achieve both stability and high gain.

inductance and cascode transistor size result in a high gain stable amplifier. This freedom is utilized to choose a pair which results in an output reflection coefficient (Γ_{out}) whose absolute value is equal to that of the input (Γ_{in}), considering the supply path impedance. Two impedances whose reflection coefficients have identical absolute values can be complex conjugate matched (i.e. $\Gamma_{in} = \Gamma_{out}^{*}$) by simply using a piece of TL [57]. This piece of transmission line can be connected to either the input or the output, or it can be broken into two pieces to be connected to both input and output nodes. In this case, two or more of this stage can be cascaded to have a higher gain using only a piece of TL as the interstage matching to have maximum power flow.

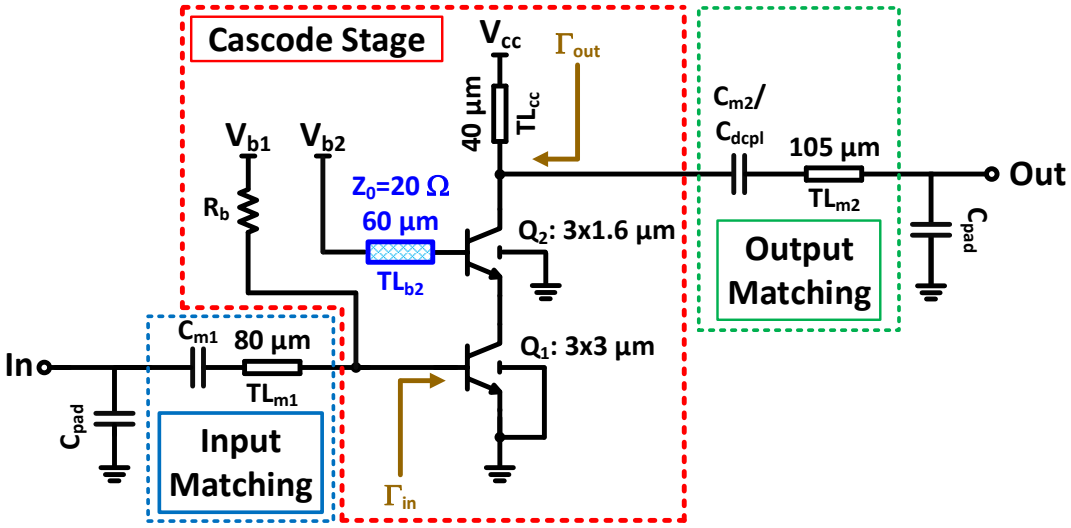

Figure 5.7: The designed desensitized unbalanced cascode amplifier at 180 GHz with input and output matching networks

5.3.1 Design Example

The above method is employed to design an unbalanced cascode amplifier at 180 GHz, depicted in Fig. 5.7. First, the main transistor size and bias current should be selected.

In each process, there is a certain current density which results in the best activity (maximum U) and hence a higher power gain (see Fig. 5.8) [7]. In this work, to keep the DC power consumption around 30 mW (with $V_{cc} \simeq 3$V), a 10 mA bias current is desired. According to Fig. 5.8, to fully utilize the employed transistor capability and the consumed DC power, the emitter length of the main transistor is selected to be 9 μm which is most active with the desired 10 mA bias current.

Based on Fig. 5.6 and output impedance considerations, a cascode transistor with total emitter length of 3×1.6 μm along with an inductance of 10 pH are selected which results in 10.7 dB power gain in simulation. The desensitized TL at the base is imple-

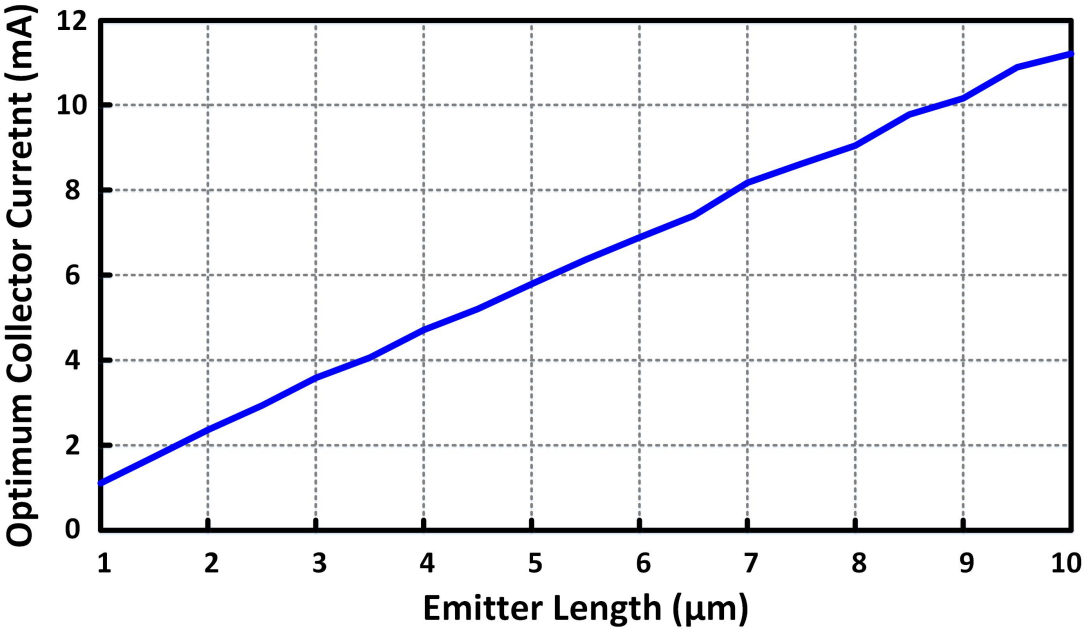

Figure 5.8: Collector current at which U (activity figure of merit) becomes maximum vs. total emitter lengths at 180 GHz [7]. To have maximum activity, current density has to be ~1.15 mA/μm

mented as a GCPW with a track of 12 μm wide and a total wall distance of 18 μm as shown in Fig. 5.9. Its ground plane is composed of first four metal layers and the signal track is thickened by connecting the remaining two thick top metal layers which results in $Z_0 \simeq 20\ \Omega$.

Considering the DC pad capacitance, the required length to provide the desired inductance with the lowered Z_0 TL is ~60 μm which is reasonably long to be fabricated without significant modeling and process variation errors. Both input and output matching networks are composed of a TL in series with a capacitor. These TL's are implemented as GCPW's with a track of 2.5 μm wide and a wall distance of 40 μm and a ground plane composed of three lower metal layers. The matching capacitance at the output serves also as a decoupling capacitor in case of cascading. Matching capacitors

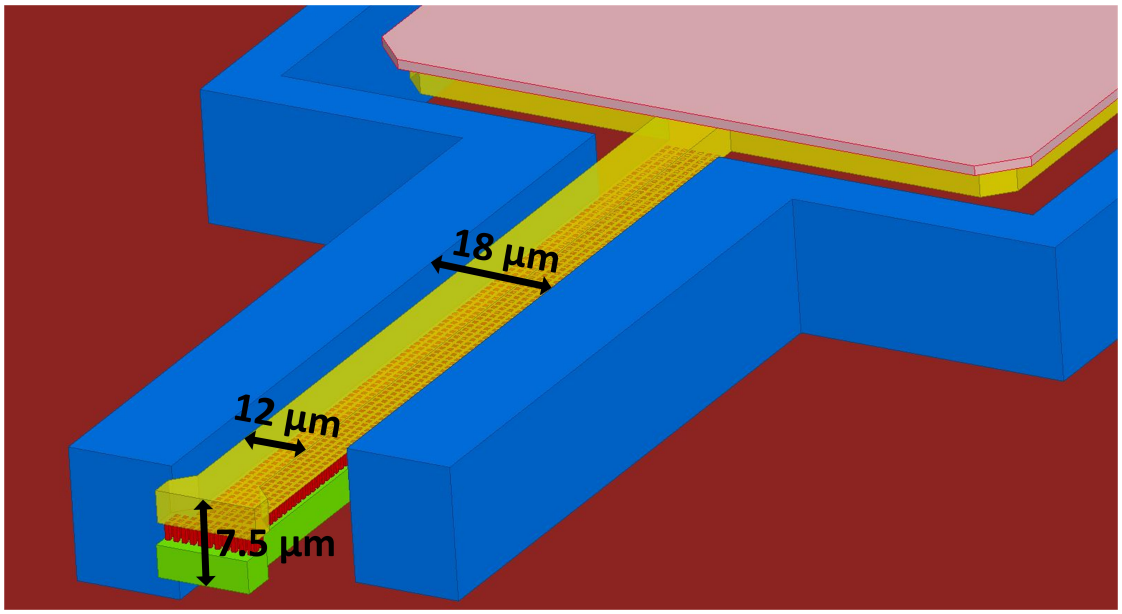

Figure 5.9: Desensitized TL for the base of the cascode transistor

are implemented as finger-caps using two top metal layers to have high quality factor and low parasitics to the ground.

5.4 Measurement Results

The die photo of the fabricated circuit in a 130 nm SiGe process is shown in Fig. 5.10. The S-parameters are measured using network analyzer connected to WR5.1 extenders and probes as shown in Fig. 5.11. The whole setup is calibrated up to the probe heads. The measured S-parameters are demonstrated in Fig. 5.12. The amplifier achieves a power gain of 9.5 dB at 183 GHz and a 8.5 GHz 3-dB bandwidth while consuming ~30 mW DC power. The large signal measurement is performed using a power meter connected to the output while the network analyzer is connected to the input as shown in Fig. 5.14. The results are shown in Fig. 5.14. The amplifier has a -2.8 dBm saturated

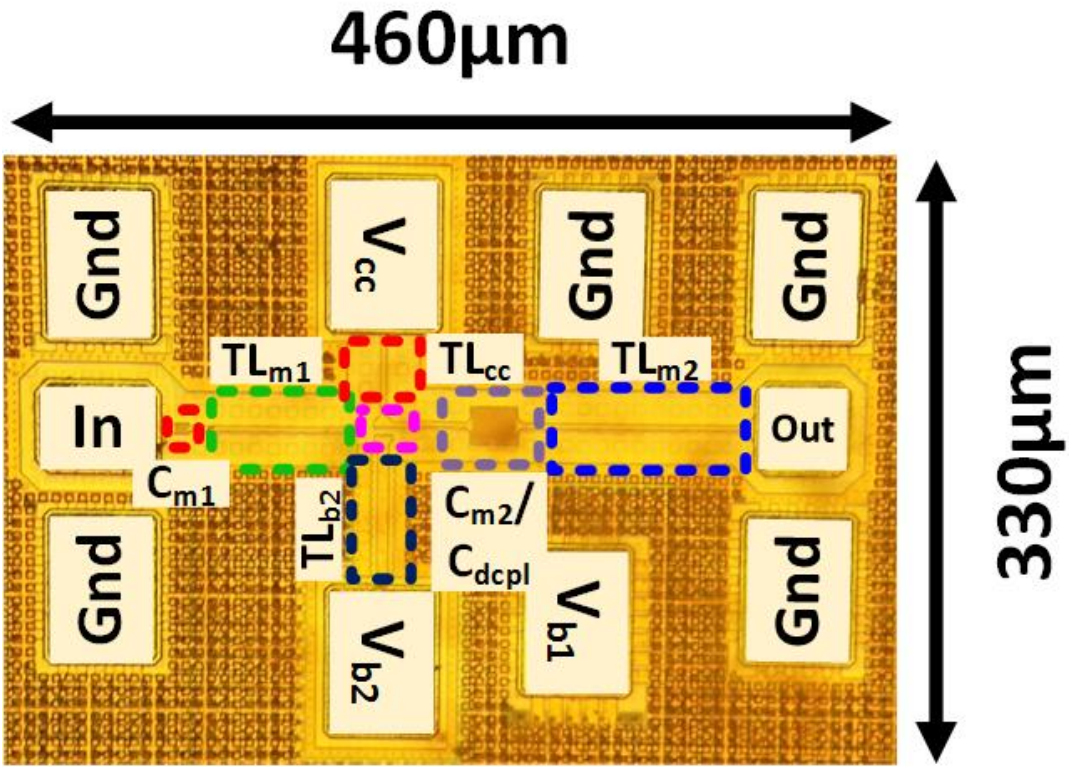

Figure 5.10: The die photo of the fabricated cascode amplifier

output power. Table 5.1 compares the results of the state of the arts with this work.

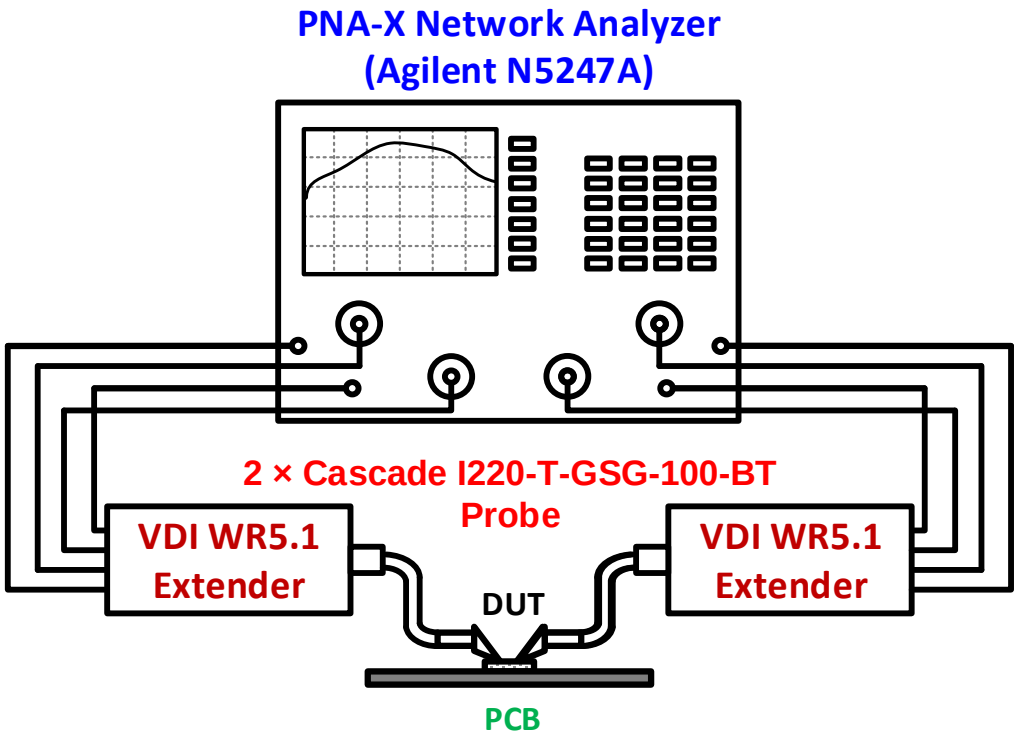

Figure 5.11: *S*-parameters measurement setup

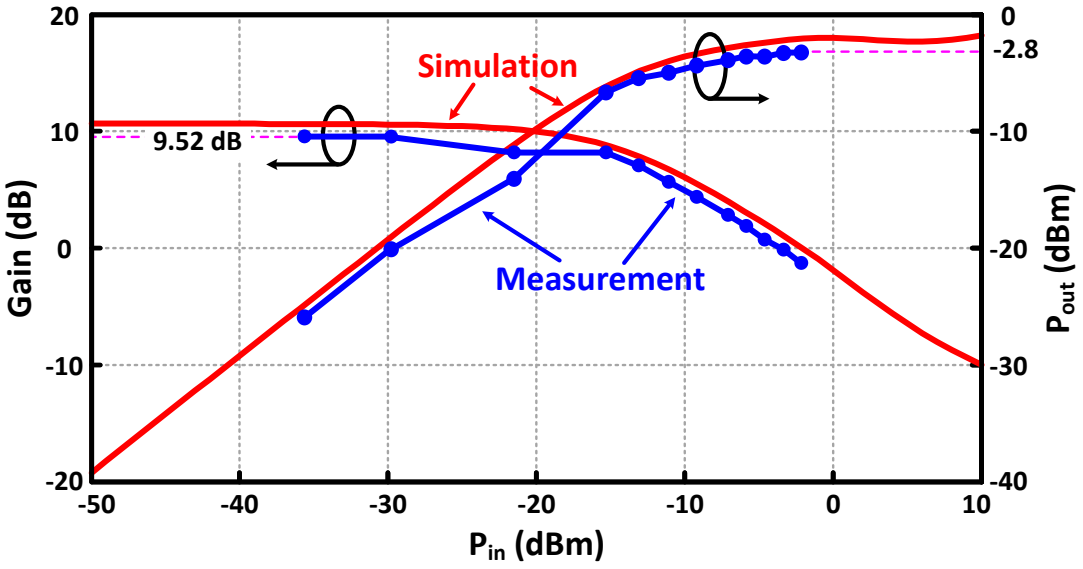

Figure 5.14: Large signal simulation and measurement: output power and gain versus input power

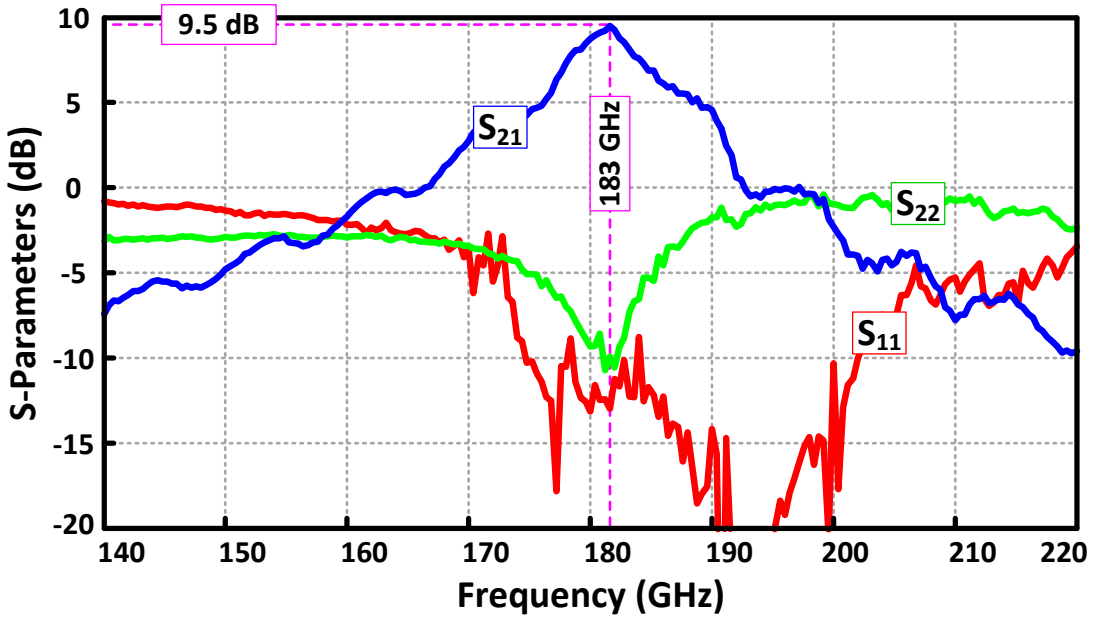

Figure 5.12: The measured S-parameters of the fabricated unbalanced desensitized cascode amplifier

5.5 Conclusion

A novel method for designing a desensitized high power gain cascode amplifier is presented based on which a single stage cascode amplifier at 183 GHz is designed and fabricated in a 130 nm process. The measurement results show a power gain of 9.5 dB, -2.8 dBm saturated output power and a 8.5 GHz bandwidth.

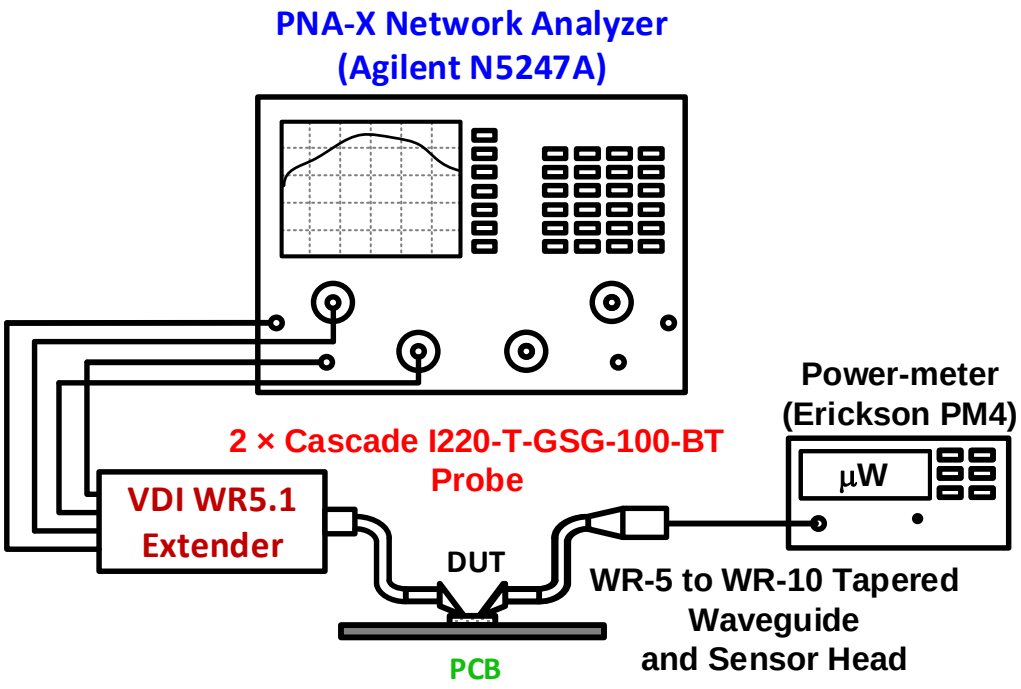

Figure 5.13: Large signal measurement setup

Table 5.1: Comparison table

	Process	Freq. (GHz)	Structure	P_{DC} (mW)	Gain dB	P_{sat} (dBm)	3-dB Bandwidth (GHz)
[72]	65nm CMOS	140	3 CS & 3 CG	63	8	-1.8	10
[37]	130nm SiGe	140	3 Cascode & 2 CE	112	18	-	~ 2
[73]	65nm CMOS	144	3 Diff. Cascode	54.6	20.6	5.7	~ 2
[86]	65nm CMOS	150	3 CS	25.5	8.2	6.3	27
[87]	130nm SiGe	170	3 Cascode & 2 CE	135	15	0	~ 13
[7]	130nm SiGe	173	3 CE	42	18.5	0.9	8.2
[88]	130 nm SiGe	200	2 Cascode	18	17	-3.5	44
[90]	40nm CMOS	213	9 CS	42.3	10.5	-3.2	~ 13
[79]	130nm SiGe	233	4 Diff. Cascode	68	22.5	-	10
This work	130nm SiGe	**183**	**1 Cascode**	**30**	**9.5**	**-2.8**	**8.5**

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